Mindway : Consulting & Design

FPGA World: from Concept to Implementation

Michele Corvo – Sales & Marketing Manager

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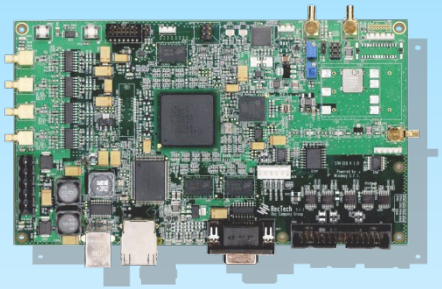
Mindway : Xilinx Expert & ATP

- 2005 Spin off of Acsis/Siscad (historical EDA/Silicon company, on the market since 1984)
- Southern Europe Xilinx Xperts Partner
- Xilinx Worldwide Broadcasting IP Core Partner
- European Xilinx Authorized Training Provider (ATP)

Business Strategy

- Customer Services
- Methodology Transfer
- Future Directions



Communication

Research

Industrial

Defence

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Board Design : Digital / Analog / RF

Board design capability: from spec to final product

- Mixed Environment (Digital&Analog) Design
- FPGA (Altera, Lattice, Microsemi, Xilinx) or Asic Design
- System on Chip Design: IP & Core Design and Integration
- UP, uC, DSP based, Hardware and Software Design
- RTOS, QNX, Linux, WinCE, Android Porting and Design
- Drivers, BSP, Interface, Protocol Development
- Analog, RF (FM-VHF-UHF-C-X-K band)& Power Design
- Signal Integrity Design and Consulting
- Industrial Bus: CAN, Profinet, Ethercat, Power Link
- Quality Design and Certification DO254/DO178/EN50128 /EN50129/ISO26262/IEC61508/IEC62304 – Gap Analysis
- FMEA/FMECA Analysis

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Xilinx Technology Training Courses

Core Design Skills	•Key for ALL Designers. Focuses on tools, architecture, and methodology. From best practice FPGA design techniques through advanced skills and methodology to meet your design goals.	Xilinx Recommended Design Methodology
Product Training	•Latest product training! Focused and in-depth training to become proficient using these products in the minimum time possible. Includes all new HW and SW products.	Vivado™ NEW; 6 series; 7 series; Zynq AP SoC NEW
Specialty Design Skills	•Focused training around specific types of FPGA design. DSP for the video and communications markets. Connectivity for high speed interfaces and Embedded design for BOM reduction, and system integration in every market and application.	DSP; Embedded for HW | SW | Firmware; Connectivity
Point Technologies	•Training required on point technology solutions such as High-Level Synthesis, AMS technology for ADC, Partial Reconfiguration, Memory, Power Optimization, and on chip Debug.	High-Level Synthesis; Agile Mixed Signal; Partial Reconfiguration; Low Power; Memory; Debug
Languages	•Focus on language skills needed to create reliable and optimal hardware using Xilinx design tools. Includes Hardware Description Languages (HDLs) such as Verilog, System Verilog, and VHDL; Tcl scripting language; and C language;	VHDL; C; Verilog; Tcl; System Verilog

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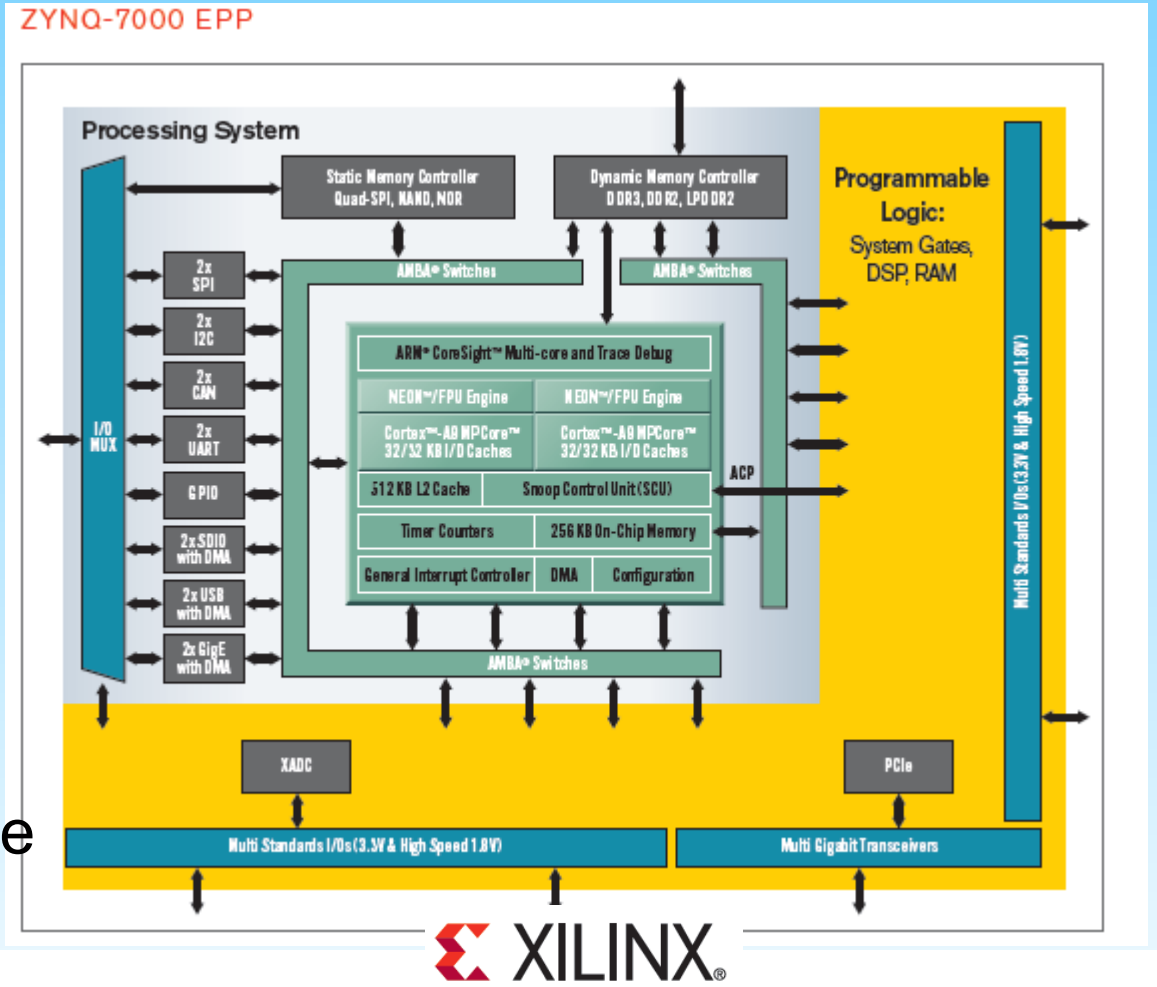
Linux Operating System Training

Course	Description
Introduction to Linux	Two-days course provides distribution-independent knpwledge for embedded Linux Software Designers
Linux Programming and GNU Tools	Three-days course introduces software design adn development for Linux, for learning concept tools and techniques required for software design cycle phases. Major topics include user application debugging, profiling and integration
Embedded Linux	Four-days course on Embedded Linux, structured to provide solid groundings to skilled developers, for methodology to adapt the Linux Kernel and User-Space Libraries and Utilities to defined Embedded Environments. The course includes extensive hand-on exercises and demostrations, focused on tools used for developing Embedded Linux Devices.
Designing with Xil Linux	Two-days intermediate-level course, for embedded developers withexperience oncreating an embedded Linux System, targeting a Zynq Xilinx SoC or a Xilinx Device with a Microblaze Processor. The course is focused on Embedded Linux Components, Open-Source Components, Environment Configuration, Network Components and Debugging Option.
Designing with Xil Kernel	Two-days course designed to allow Xil-Kernel users to bring-up their boards. The course offers hands-on experience to students, in order to build Environment and Booting the System, using a Microblaze with Xil-Kernel RTOS

SoC FPGA Advanced Architecture Experties

- Dual Arm Cortex 9 Processing System
- Powerful Logic FPGA along with 7 Series
- Best-in-class tools, operating system, ecosystem ARM leveringing
- Cost Effective, Scalable Size Solution



FPGA - IP Core List Xilinx Spartan-Virtex-7 Series

Networking	Audio-Video	Transport Stream	Broadcasting
GBE IP Hardware Protocol Stack	H263 Compressor	TS Demultiplexer	DVB-T/H Mod.
Data over IP Video over IP IP2TS / TS2IP	Image recognition	TS Multiplexer	ISDB-T/Tb Mod.
Band Rate Equalizer	MPE2 Audio Encoder	TS Analyser	8/16 VSB Mod.
NCR Synchronizer	Audio Echo Canceller	MPE Decapsulator	DVB-C/J83 Mod.
		ES/PS/PES Man.	DVB-S/S2 Mod.
		PCR Restamping	DVB-SFN
			F-SIM
Queu Manager			Digital PAL/NTSC
Traffic Manager	Legenda :		Digital FM
Packet Analyzer	Available		*DAB / DAB +*
10 Gigabit IP Stack	Under development		*DMB-T*
			DVB-T2

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FPGA - IP Core List Xilinx Spartan-Virtex-7 Series

Telecom	Peripheral	Industrial	FEC / Encryption	Pre-Distorsion
TDM Switch Matrix	VME Mast./Sl.	Sensor interf.	Reed Solomon	Linear Pre-Dist.
Utopia Mux/Demux	VSB	PID Motor CTRL	Trellis	Non-Linear Pre-D.
IEEE 802.4 (Token)	ARINC 429	Ethernet Interf.	MPEG II COP3	Group Delay Pre-Distorsion
FSK Modem	X86 Peripherals		Turbocode	
QAM Modem	IIC M/S		*BCH/ LDPC*	
	SDRAM CTRL		*RSA Encryption*	*Adaptive Linear-Non Linear Pre-Distorsion*
	ASI Interface		*AES Encryption*	
	ASI Ser/Des			

Legenda :

Available

Under development

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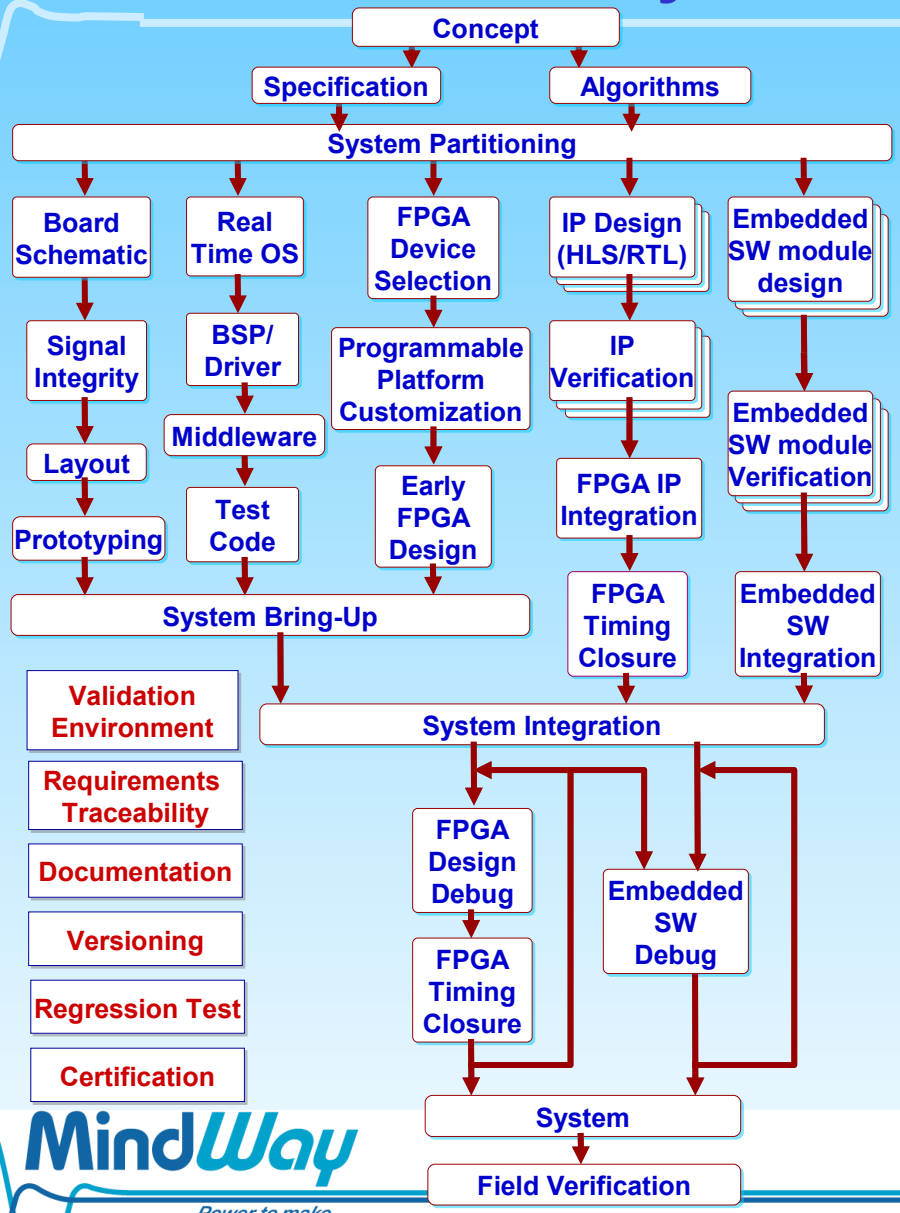
FPGA Centric System Design Methodology



- FPGA World is a complex environment with System, IP Core, Hardware & Software Tasks
- Modern FPGA is a SoC that requires dedicated Methodology to match Time Schedule and Design Constraints
- FPGA needs different Skills and Awareness Convergence

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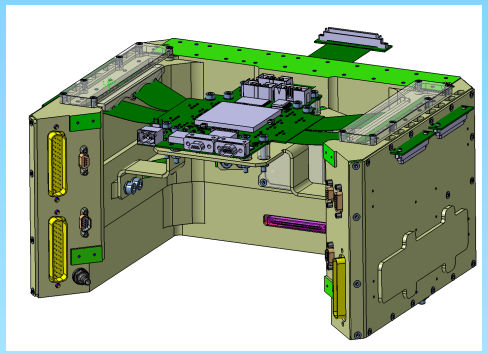
FPGA Centric System Design Methodology

Cherenkov Telescope



Weather Satellite Test System

Residential Modem-Router for 2-ways Satellite access network (Smart-LNB)

Audio, Video, Telemetry IP radio Link for Racing Cars

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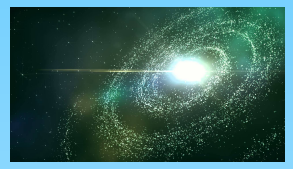
Cherenkov Telescope Array – CTA Project ASTRI



SiPM

Shaping
A/D
conversion

8x8 pixels

CITIROC

FRONT-END
FPGA

Internal
Connectivity
(mini Flat,
10 couples)

Trigger

Data /
Housekeeping

37 modules

Trigger Detection
Logic

BACK-END
FPGA A1

BACK-END
FPGA A2

Trigger Algorithm
Variance Algorithm
Fast Differential Link

BACK-END
FPGA ZynQ

Camera
Server

Data Packing HW

GBE IP stack

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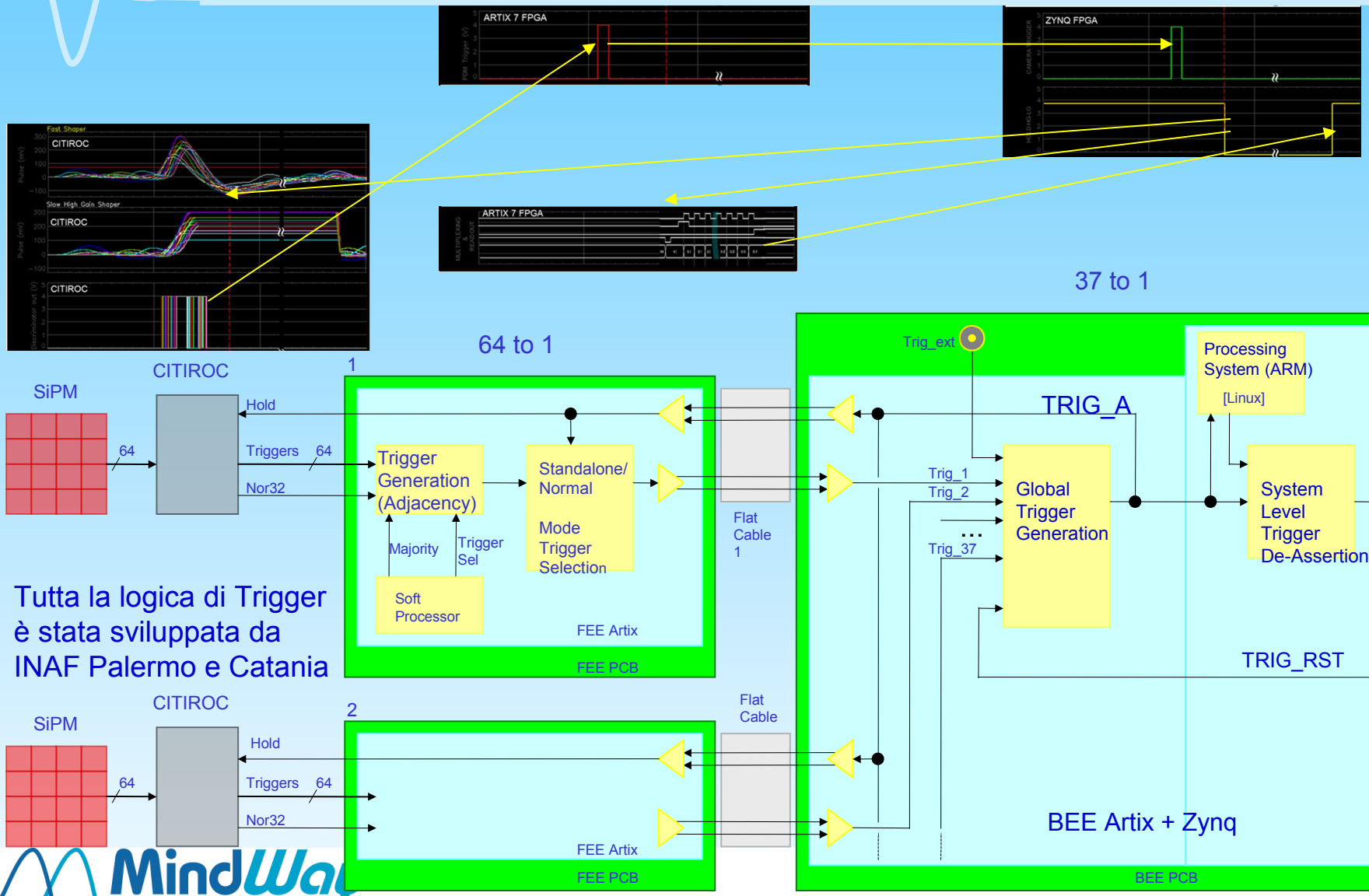

Tutta la logica di Trigger è stata sviluppata da INAF Palermo e Catania

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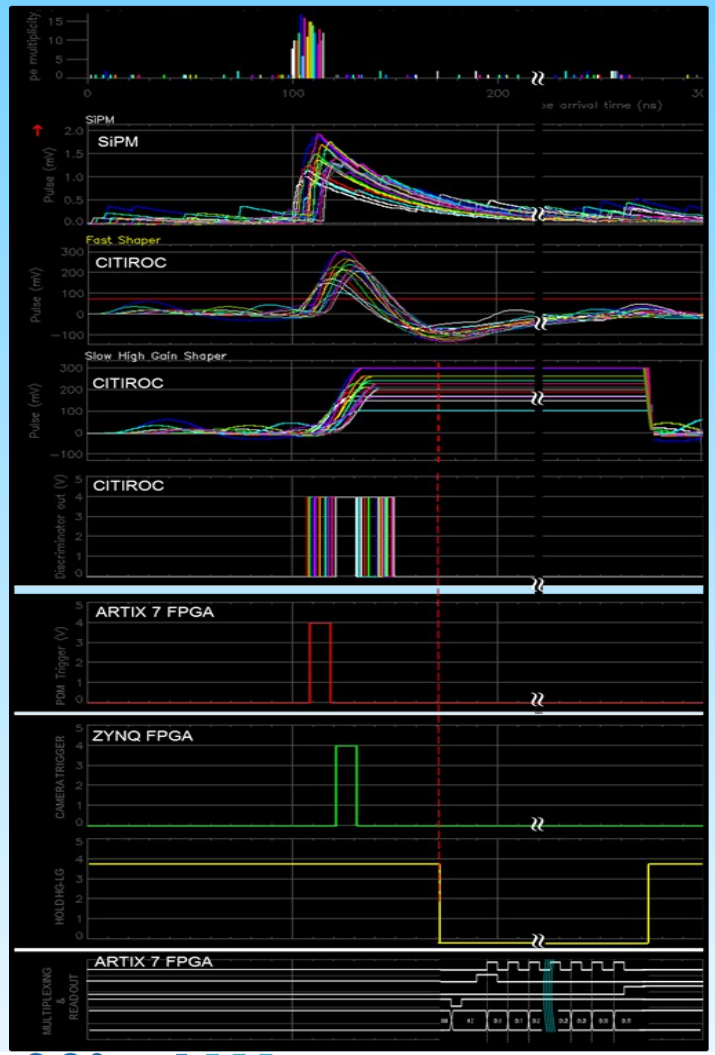
Cherenkov Telescope Array – CTA Project ASTRI



converted photo-electrons (pe) at different pixels and at different time

related SiPM signals

fast shaper (15 ns shaping time) and threshold (red line)

slow shapers (40 ns shaping time)

digital triggers from discriminators

PDM trigger generated if ≥ 4 adjacent pixels are over a given threshold in pe

camera trigger sent to all the PDMs. This signal activates the peak detector.

HOLD signal sent to the CITIROCs holds analog memories values

conversion of analog values to digital performed in 6.4 µs

Immagini gentilmente offerte
da INAF Palermo
Osvaldo Catalano

Tutta la logica di Trigger è stata sviluppata da INAF Palermo e Catania

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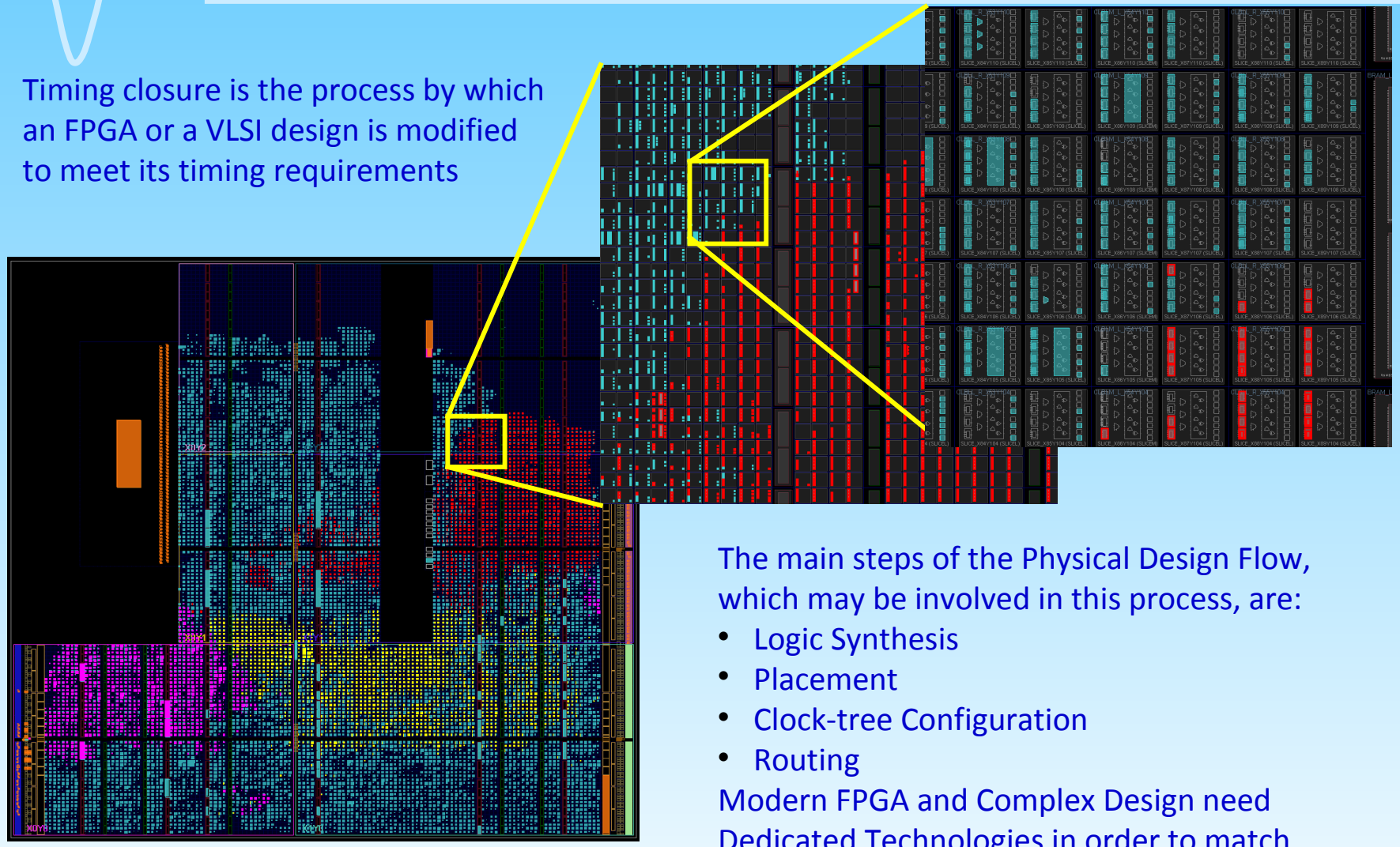
Timing closure is the process by which an FPGA or a VLSI design is modified to meet its timing requirements



The main steps of the Physical Design Flow, which may be involved in this process, are:

- Logic Synthesis
- Placement
- Clock-tree Configuration
- Routing

Modern FPGA and Complex Design need Dedicated Technologies in order to match Timing and Area Constraints

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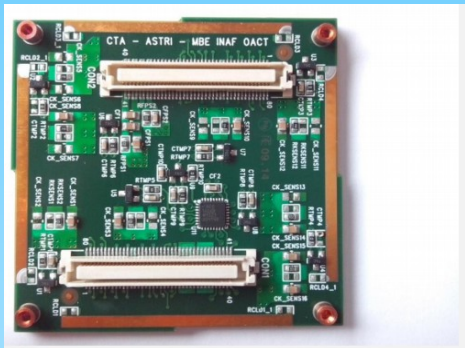
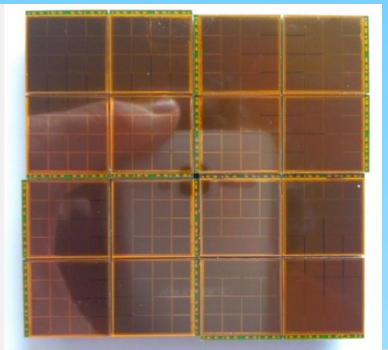
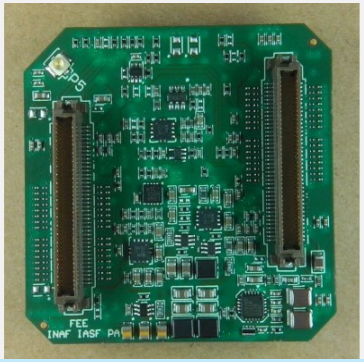
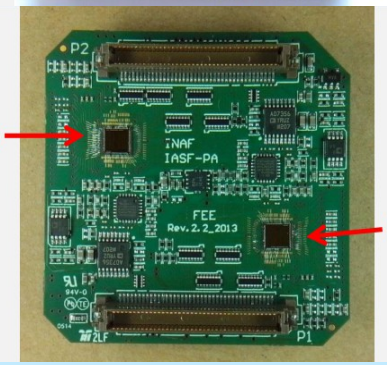
PMD





FEE SIPM board

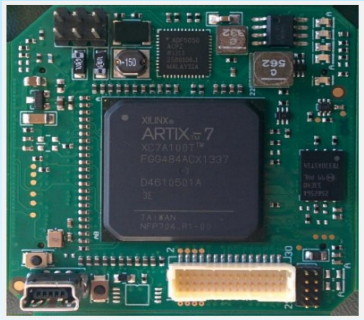


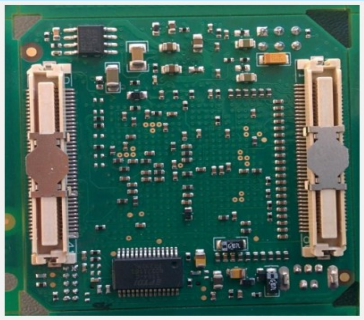


CITIROC

CITIROC

FEE asic board





FEE FPGA board (Mindway Design)

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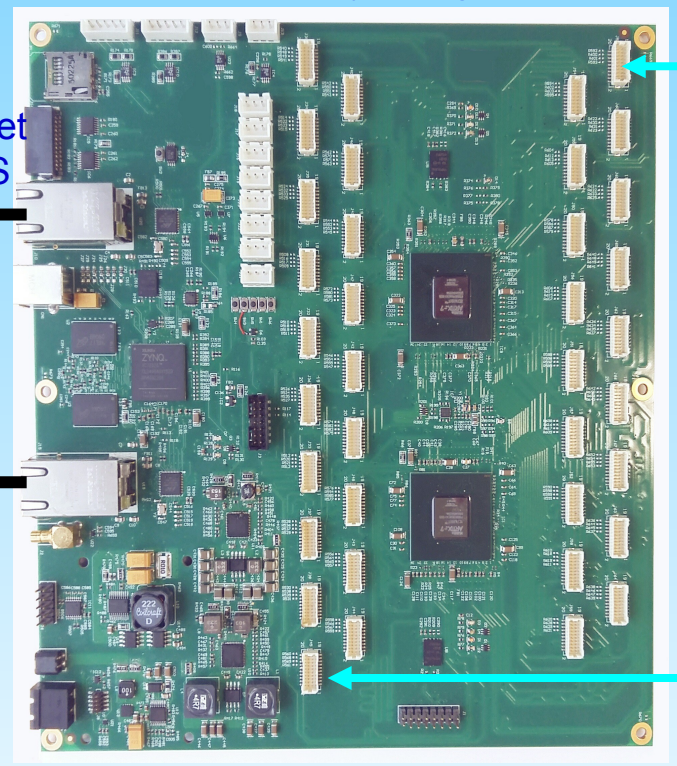

Embedded Zynq MPSoC runs open-source Xilinx Linux kernel and Debian Wheezy distribution.

Trigger/command signals routing: board breakout relies on Xilinx 7 Series devices with largest pin-count.

High performance custom data manager and packet-maker, fully-hardware IP/UDP stack to communicate with remote server.

GPS (event time tagging), thermal/voltage/humidity sensing capability.

M2M interoperability by means of OPC-UA protocol.

Back-End board has been designed in Mindway

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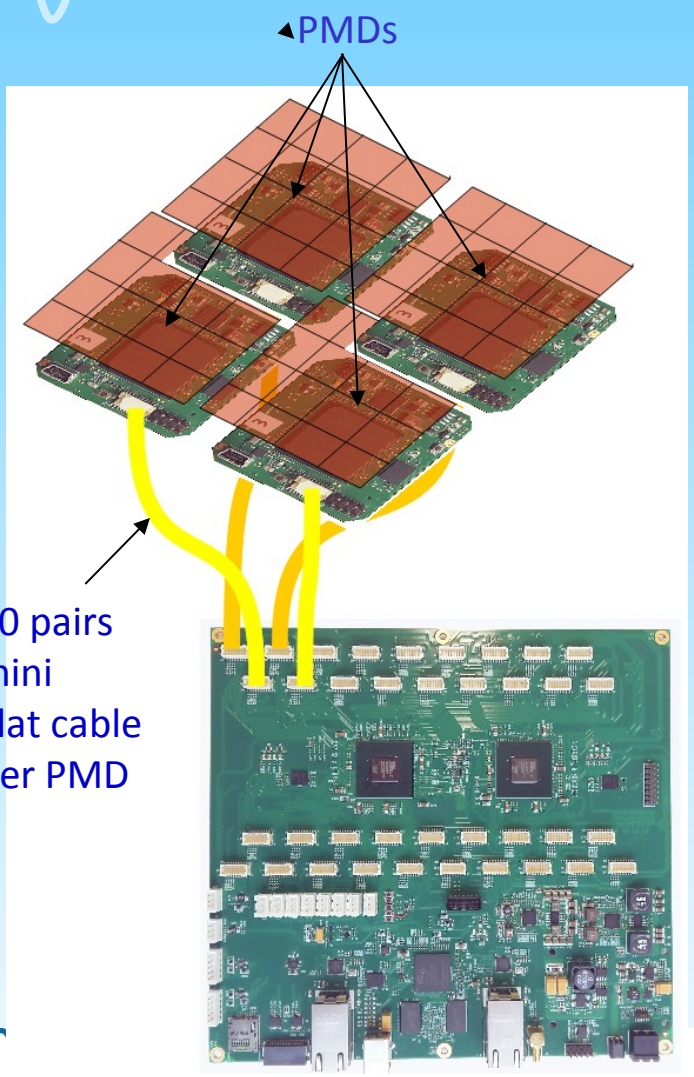
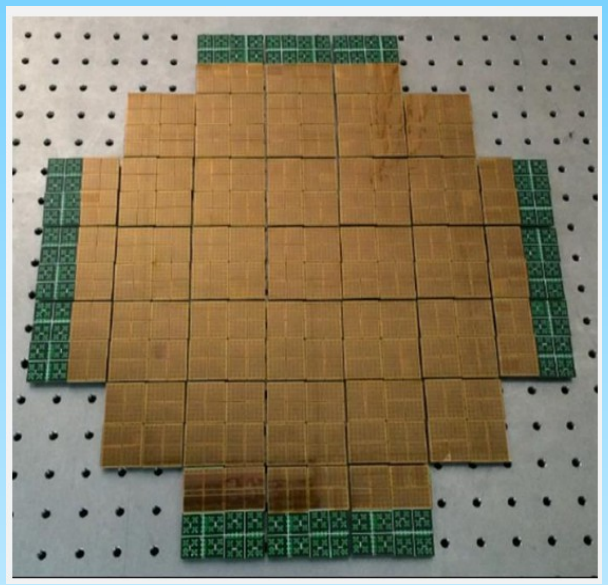
Cherenkov Telescope Array – CTA Project ASTRI

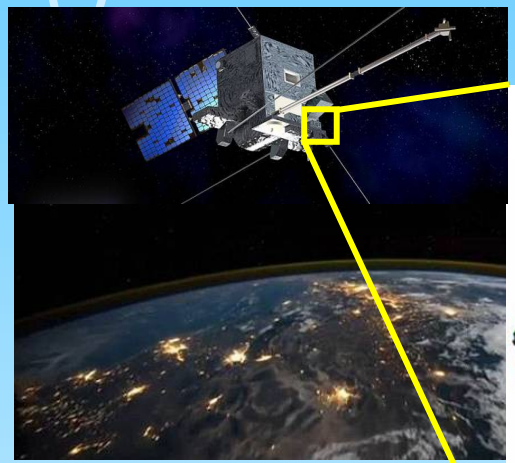


Up to 37 PDMs
To achieve the
Camera
focal plane

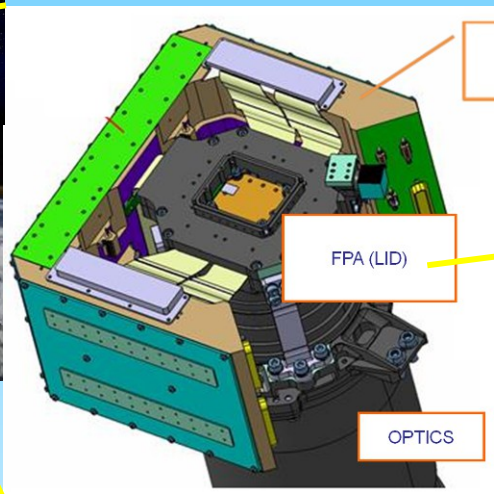


Immagini gentilmente offerte
da INAF Palermo
Osvaldo Catalano

Lightining Imager Module for Weather Satellite

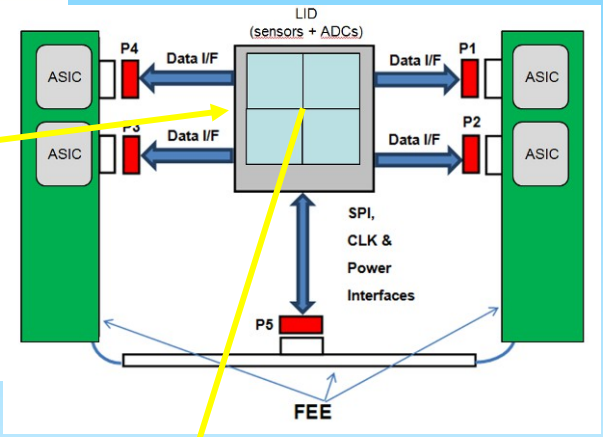


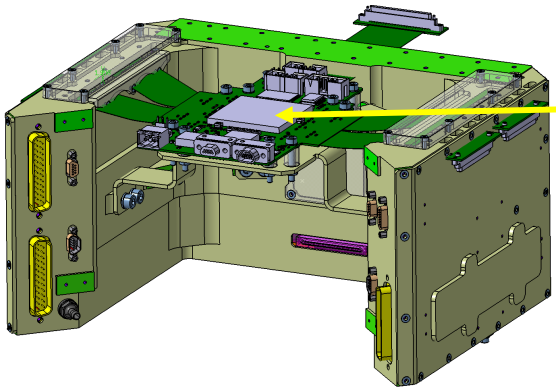
Lightning Imager (LI) Module for weather satellite

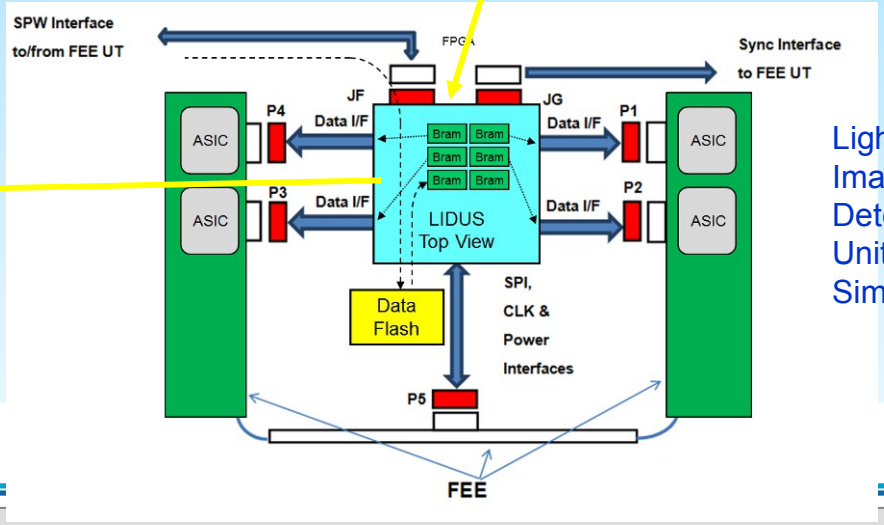


Focal Plane Assembly

Lightning Imager Detector

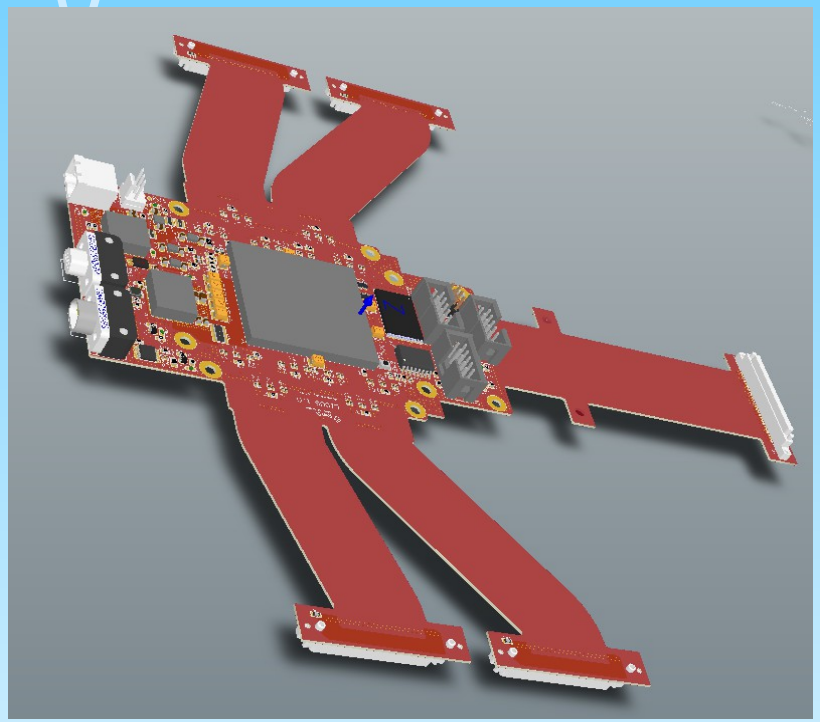




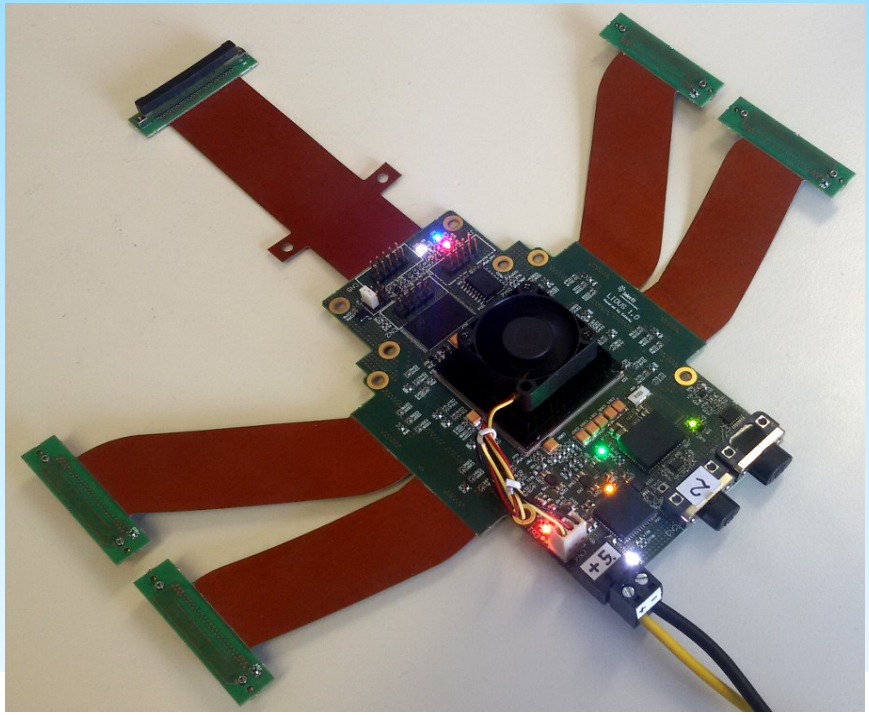


Lightning Imager Detector Unit Simulator

Lightining Imager Module for Weather Satellite



Mechanical and PCB design 3-D visualization



Prototype photo with FAN cooler

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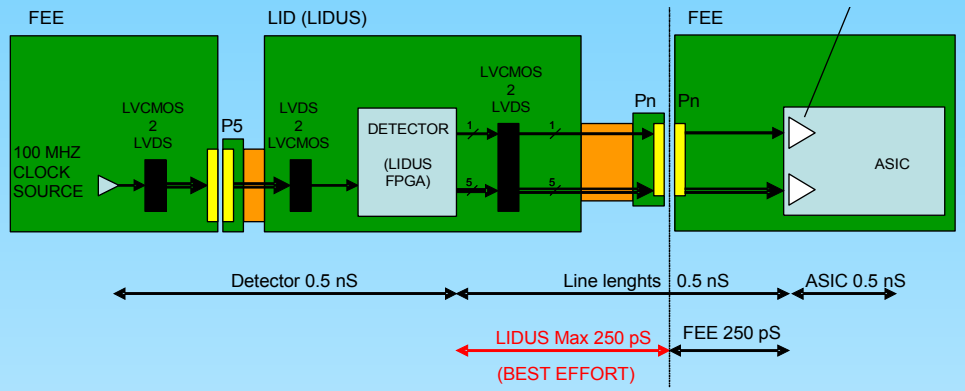
Lightining Imager Module for Weather Satellite

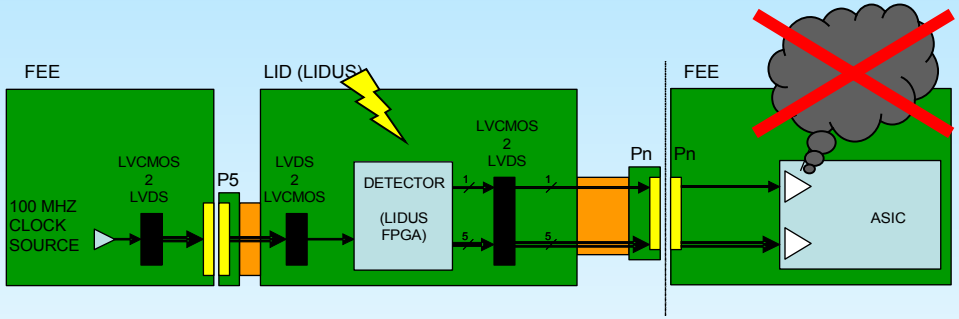
LIDUS Functional requirements:



Detector to connector
PCB SKEW < 100 pS

Buffer to ASIC receiver
Signal integrity analisys:
- Propagation
- Crosstalk

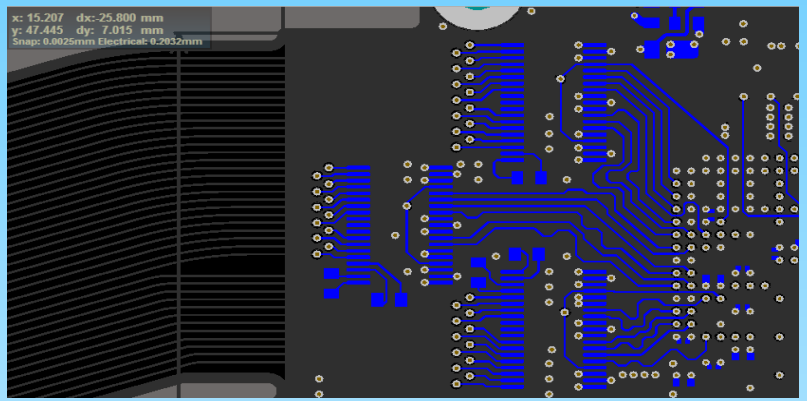
FEE protection requirement:



Single Failure on LIDUS shall NOT damage or derate FEE
(FMEA analisys)

Lightining Imager Module for Weather Satellite

Impacts on
Top/Bottom
Orientation
Placement
FPGA bank
Pins in bank



Compensation of
FPGA package delay

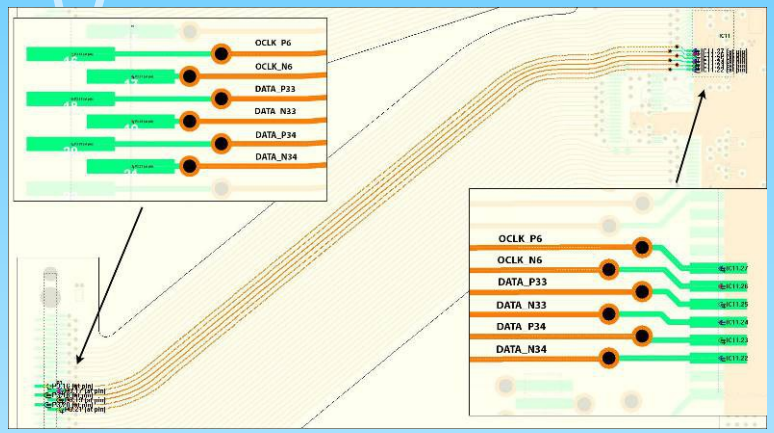
Hand correction
According to
excel analisys

Worst (overall)
PCB Skew <= 1 pS

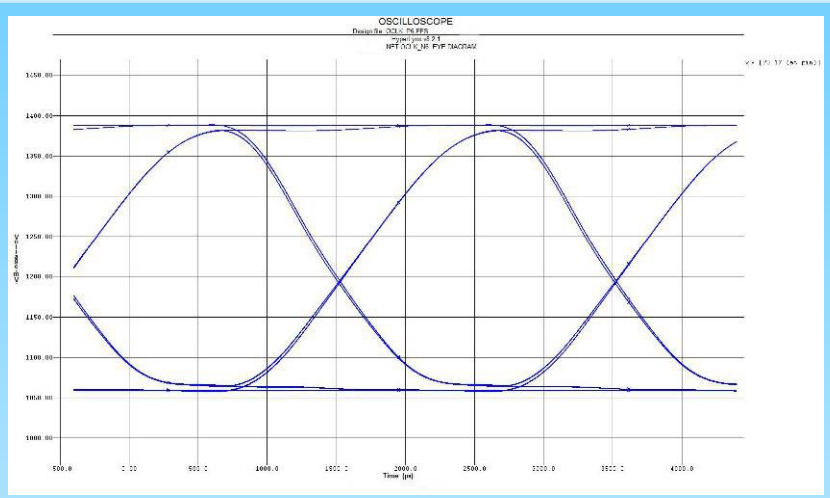
P1			PIN	FPGA Delay (ps)	Board Initial Length (mm)	Board Initial Delay (ps)	IN. Board+FPGA Delay (ps)	Max Delay (ps)	Constraint (ps)	Constraint (mm)	Actual length (mm)	Delta (mm)	Delta (ps)	Diff Length	Delta tracks pair (mm)	Av. Track Length (mm)	Skew pair tracks (mm)	Skew pair tracks (ps)	Average Pair Length (mm)	Skew Pair (mm)	Skew Pair (ps)	Total Skew (ps)	Optimal Length (mm)	Net Name
7	DATA_P15	LVDS+	C15	69.29	9.871	65.72435686	135.0143569	146.0243027	76.73430266	11.52456011	11.525	0.000439886	0.00292891	90.112	1.805		-0.974	-5.988094125	91.015	-0.072	-0.441001543	-0.438072637	11.59079319	N16786631
8	DATA_N15	LVDS-												91.917			0.831	5.106091039						
9	DATA_P16	LVDS+	B14	85.58	9.078	60.44430266	146.0243027	146.0243027	60.44430266	9.078	9.078	0	0	90.226	1.752		-0.860	-5.287408746	91.102	0.016	0.096805217	0.096805217	9.063461032	N16788603
10	DATA_N16	LVDS-												91.978			0.892	5.48101918						
11	DATA_P17	LVDS+	A14	87.38	7.871	52.40770062	139.7877006	146.0243027	58.64430266	8.807661866	8.809	0.001338134	0.00890974	90.329	1.758	91.08625	-0.757	-4.65433336	91.208	0.122	0.748319692	0.757229428	8.695273339	N16788607
12	DATA_N17	LVDS-												92.087			1.001	6.150972744						
13	OCLK_P3	LVDS+	B13	83.74	9.078	60.44430266	144.1843027	146.0243027	62.28430266	9.354345648	9.316	-0.03834565	-0.2553179	90.418	1.755		-0.668	-4.107307056	91.296	0.209	1.286126452	1.030808544	9.161185079	N16788611
14	OCLK_N3	LVDS-												92.173			1.087	6.679559959						
15	DATA_P18	LVDS+	A13	85.67	7.249	48.26622053	133.9362205	146.0243027	60.35430266	9.064483093	9.022	-0.04248309	-0.2828664	90.162	1.677		-0.924	-5.680775976	91.001	-0.086	-0.527050625	-0.809916999	9.143639695	N16788615
16	DATA_N18	LVDS-												91.839			0.753	4.626674727						
17	DATA_P19	LVDS+	C12	74.15	9.456	62.96115069	137.1111507	146.0243027	71.87430266	10.79464715	10.982	0.187352848	1.24745674	90.066	1.662		-1.020	-6.270826822	90.897	-0.189	-1.163199192	0.084257545	10.96934554	N16788622
18	DATA_N19	LVDS-												91.728			0.642	3.944428437						
19	DATA_P20	LVDS+	A11	86.52	19.915	132.6006045	219.1206045	227.307367	140.787367	21.14455229	21.142	-0.00255229	-0.016994	79.348	1.733		-0.895	-5.499458269	80.215	-0.028	-0.173634754	-0.19062871	21.17063012	N16788636
20	DATA_N20	LVDS-												81.081			0.838	5.152188761						
21	DATA_P21	LVDS+	B11	85.13	21.122	140.6372065	225.7672065	227.307367	142.177367	21.3533134	21.316	-0.0373134	-0.2484449	79.437	1.723		-0.806	-4.952431964	80.299	0.056	0.342659736	0.094214872	21.30185007	N16788626
22	DATA_N21	LVDS-												81.160			0.917	5.637751436						
23	DATA_P22	LVDS+	A10	88.5	19.496	129.810765	218.310765	227.307367	138.807367	20.84718034	20.737	-0.11018034	-0.7336168	79.558	1.644	80.24275	-0.685	-4.208722045	80.380	0.137	0.843588318	0.109971474	20.72048362	N16788628
24	DATA_N22	LVDS-												81.202			0.959	5.89589868						
25	OCLK_P4	LVDS+	B10	89.46	20.703	137.847367	227.307367	227.307367	137.847367	20.703	20.703	0	0	79.457	1.655		-0.786	-4.829504705	80.285	0.042	0.256610654	0.256610654	20.6644602	N16788630
26	OCLK_N4	LVDS-												81.112			0.869	5.342726013						
27	DATA_P23	LVDS+	B8	89.45	20.481	136.3692182	225.8192182	227.307367	137.857367	20.70450188	20.699	-0.00550188	-0.0366333	79.357	1.673		-0.886	-5.444141002	80.194	-0.049	-0.302708376	-0.339341689	20.749965	N16788632
28	DATA_N23	LVDS-												81.030			0.787	4.838724249						
29	DATA_P24	LVDS+	A8	94.12	19.289	128.4324911	222.5524911	227.307367	133.187367	20.00312461	20.135	0.131875392	0.87806963	79.258	1.655		-0.985	-6.052630936	80.086	-0.157	-0.966515577	-0.088445949	20.14828351	N16788634
30	DATA_N24	LVDS-												80.913			0.670	4.119599782						
31	DATA_P25	LVDS+	A7	92.32	13.805	91.91821968	184.2382197	203.1771086	110.8571086	16.64939105	16.783	0.133608953	0.88961225	89.900	1.760		-1.027	-6.310265984	90.780	-0.147	-0.901466569	-0.011854319	16.78478037	N16788660
32	DATA_N25	LVDS-												91.660			0.733	4.507332846						
33	DATA_P26	LVDS+	B7	88.99	14.912	99.2889889	188.2789889	203.1771086	114.1871086	17.14951659	17.253	0.103483405	0.68902647	90.007	1.748		-0.920	-5.652605146	90.881	-0.046	-0.280683909	0.408342556	17.19167191	N17027663
34	DATA_N26	LVDS-												91.755			0.828	5.091237328						
35	DATA_P27	LVDS+	A6	101.54	13.649	90.87952049	192.4195205	203.1771086	101.6371086	15.26465905	15.261	-0.00365905	-0.0243631	90.117	1.752	90.9266667	-0.810	-4.976505219	90.993	0.066	0.407708744	0.383345597	15.20342615	N16788652
36	DATA_N27	LVDS-												91.869			0.942	5.791922707						
37	OCLK_P5	LVDS+	C7	74.13	17.637	117.432933	191.562933	203.1771086	129.0471086	19.38130808	19.385	0.00369192	0.02458201	90.239	1.658		-0.688	-4.226648937	91.068	0.141	0.868685967	0.893267981	19.250842	N16788654
38	OCLK_N5	LVDS-												91.897			0.970	5.96402087						
39	DATA_P28	LVDS+	A5	104.69	14.627	97.39136539	202.0813654	203.1771086	98.48710856	14.79156731	14.709	-0.08256731	-0.5497603	90.131	1.657		-0.796	-4.890456138	90.960	0.033	0.201805584	-0.347954684	14.76125857	N16788656
40	DATA_N28	LVDS-												91.788			0.861	5.294067306						
41	DATA_P29	LVDS+	A4	107.71	14.338	95.46710856	203.1771086	203.1771086	95.46710856	14.338	14.338	0	0	90.042	1.673		-0.885	-5.437482442	90.879	-0.048	-0.296049816	-0.296049816	14.38246309	N16788658
42	DATA_N29	LVDS-												91.715			0.788	4.845382809						
43	DVAL_P1	LVDS+	A3	106.11	13.924	92.71056072	198.8205607	192.1695928	86.05959275	12.92510541	13.924	0.998894595	6.65096797	89.925	1.663	90.7565	2.506	15.40551732	90.757	3.338	20.51621813	27.1671861	9.843818666	N16788674
44	DVAL_N1	LVDS-												91.588			4.169	25.62691895						

MindWay
Power to make

Lightining Imager Module for Weather Satellite



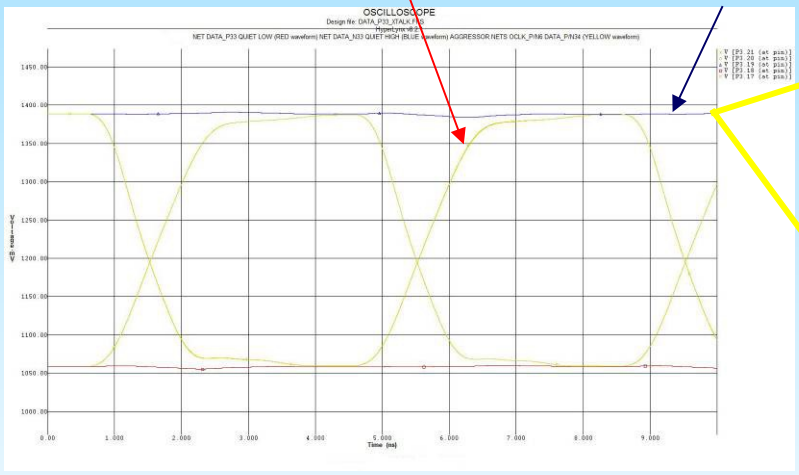
Crosstalk analisys topology



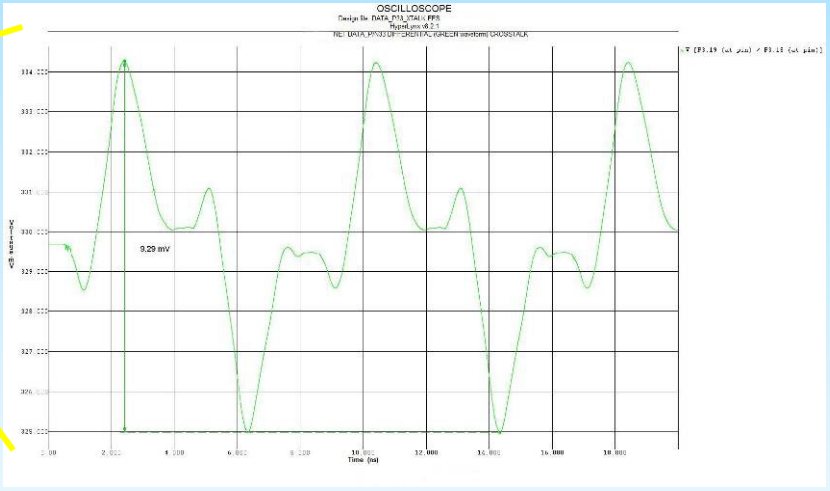
Propagation and eye diagram @ 300 MHz

Aggressor

Victim



Crosstalk Analisys



Worst differential crosstalk <= 10 mV

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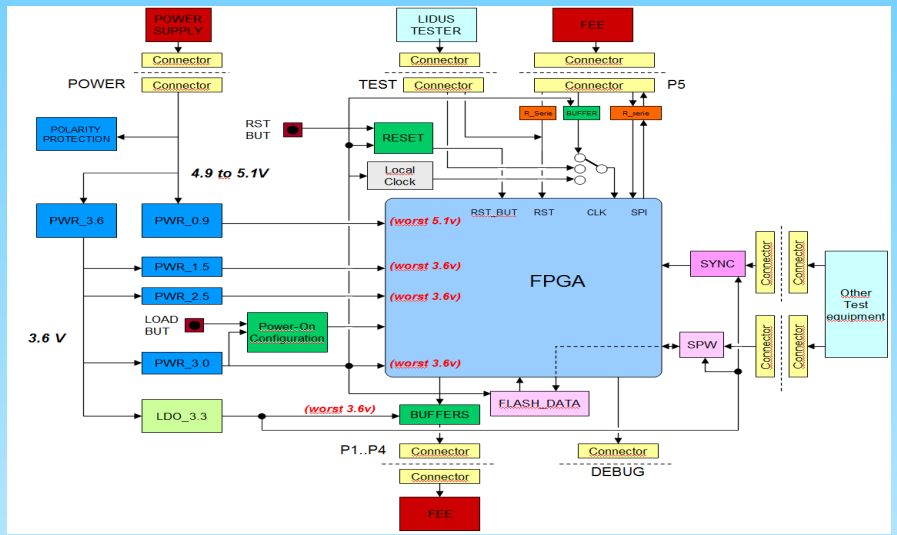
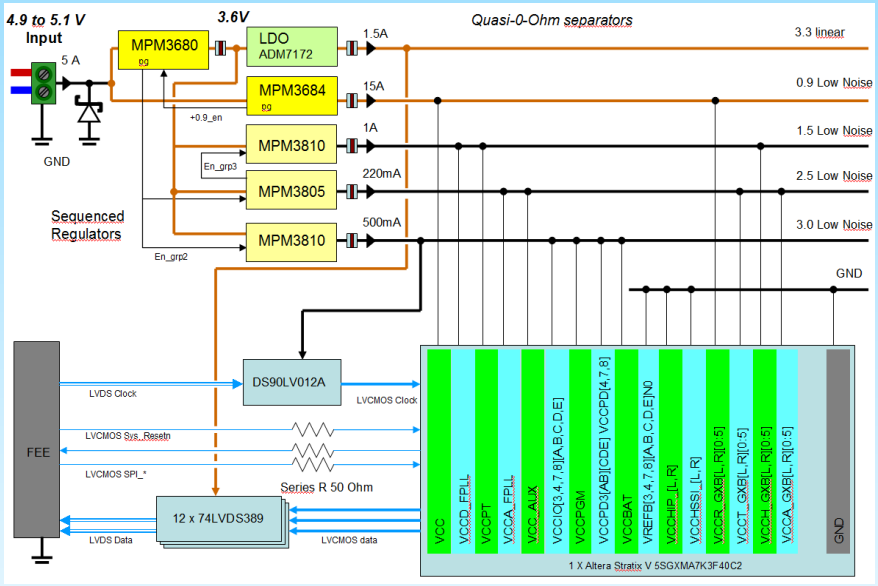
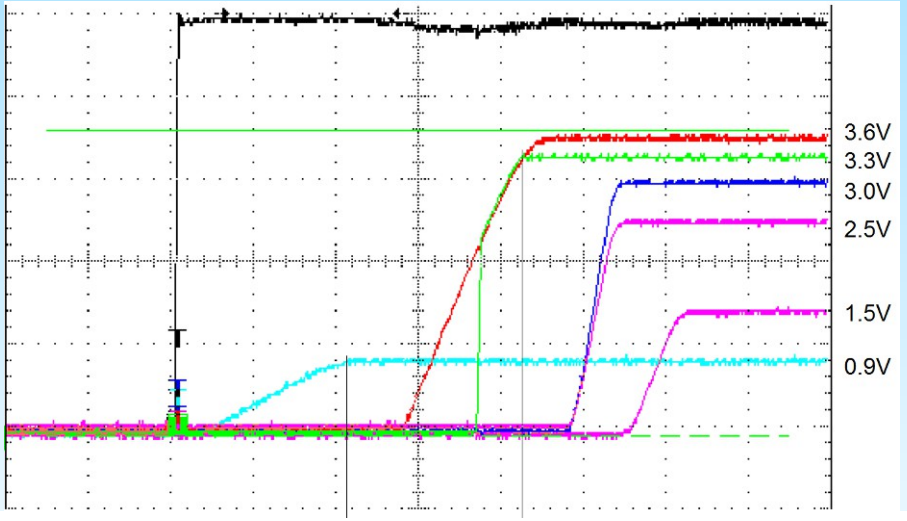
Lightining Imager Module for Weather Satellite

FMEA analisys

Power supply chain redesigned to avoid FEE damages under Single fault







"Protected" chain of sequenced Point of Loads

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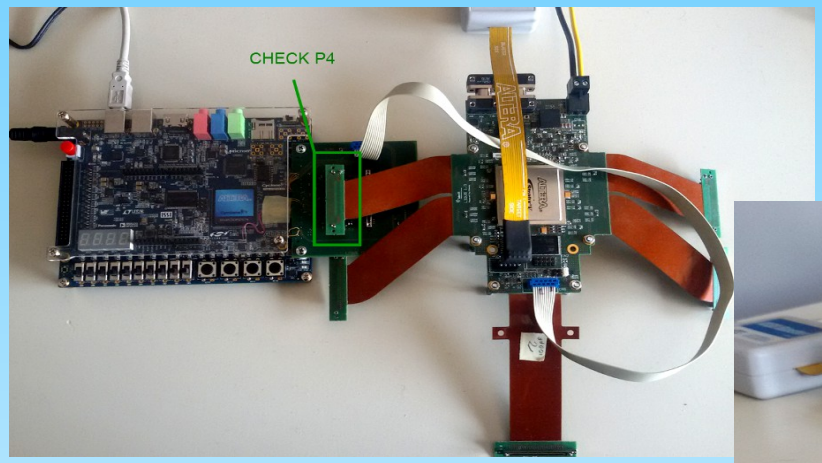
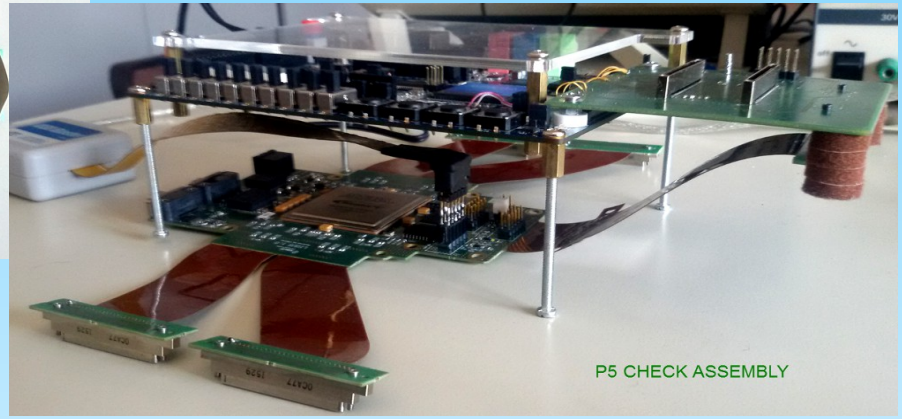
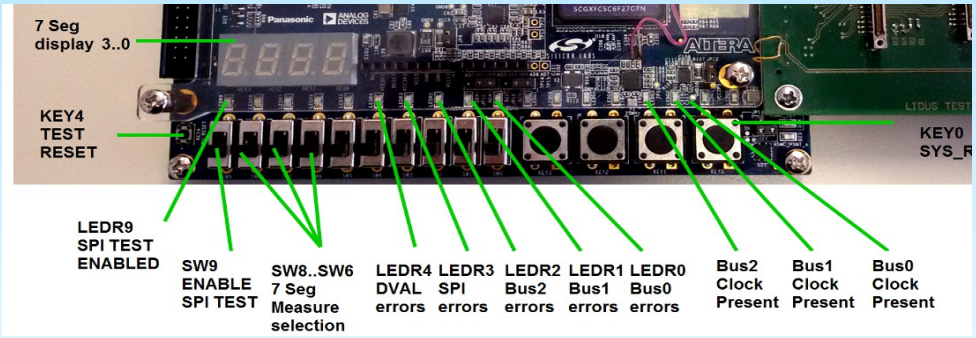
Lightining Imager Module for Weather Satellite



Lightining Imager Test Equipment :

- Data are sent from LIDUS Board (FPGA) to service board
- Service board measures delay between received lines
- Process is repeated for all design configuration with cross reference verification

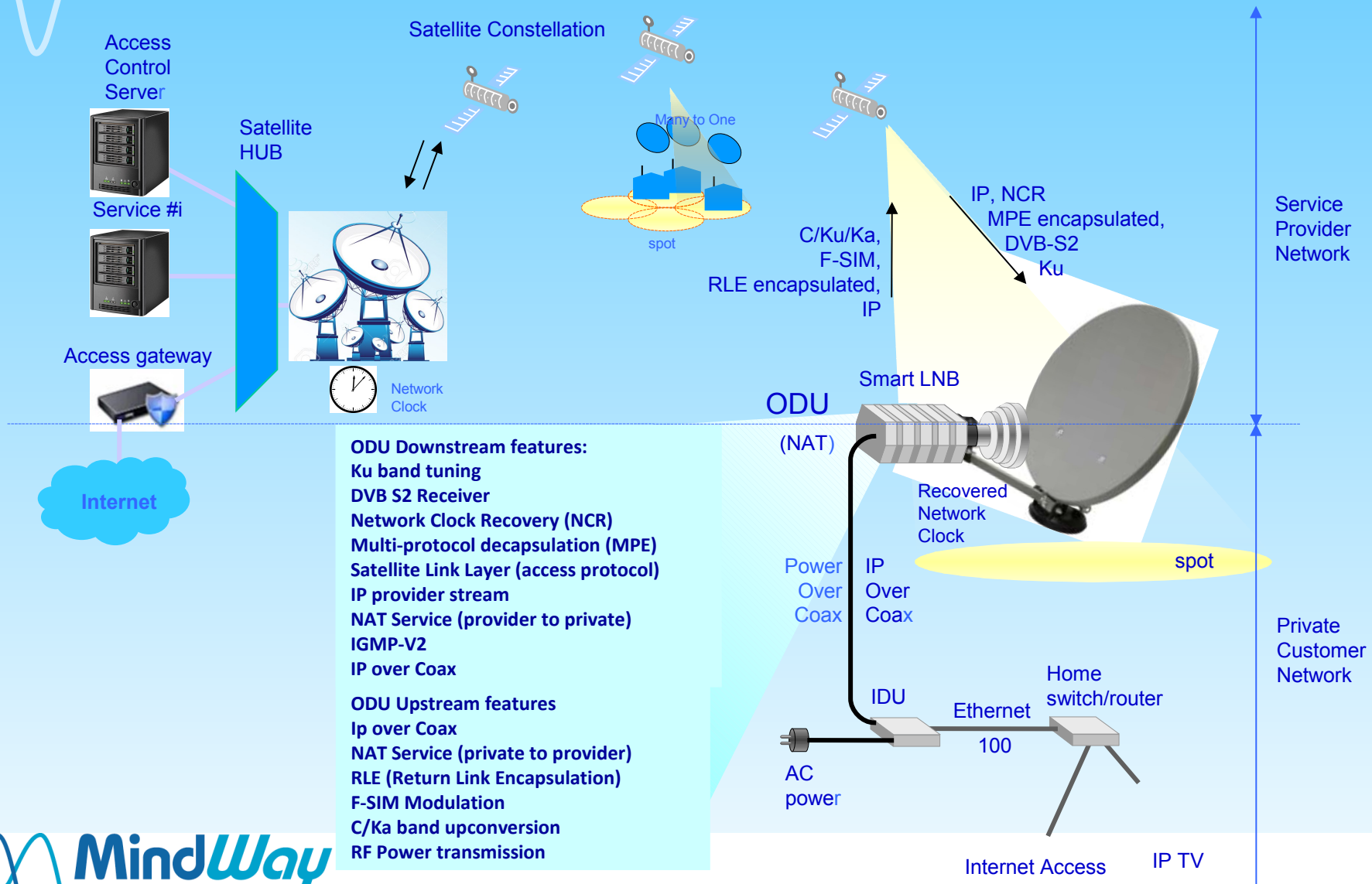




Lightining Imager Test Equipment :

- Errors are registered and stored for survey
- Errors are visualized for immediate check

Eutelsat Smart LNB- Satellite IP Modem-Router



ODU Downstream features:
Ku band tuning
DVB S2 Receiver
Network Clock Recovery (NCR)
Multi-protocol decapsulation (MPE)
Satellite Link Layer (access protocol)
IP provider stream
NAT Service (provider to private)
IGMP-V2
IP over Coax

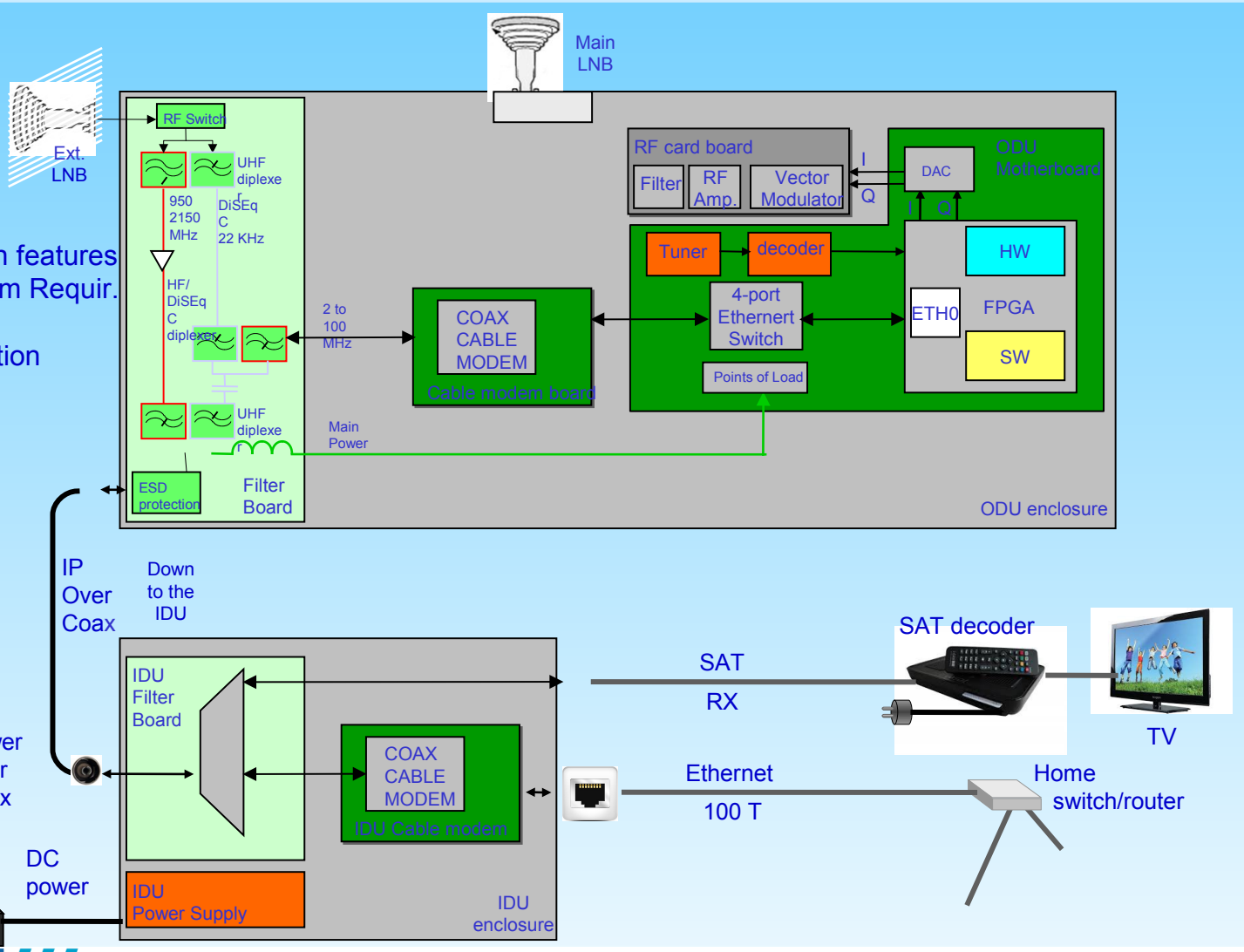
ODU Upstream features
Ip over Coax
NAT Service (private to provider)
RLE (Return Link Encapsulation)
F-SIM Modulation
C/Ka band upconversion
RF Power transmission

MindWay
Power to make

Eutelsat Smart LNB- Satellite IP Modem-Router

Smart LNB

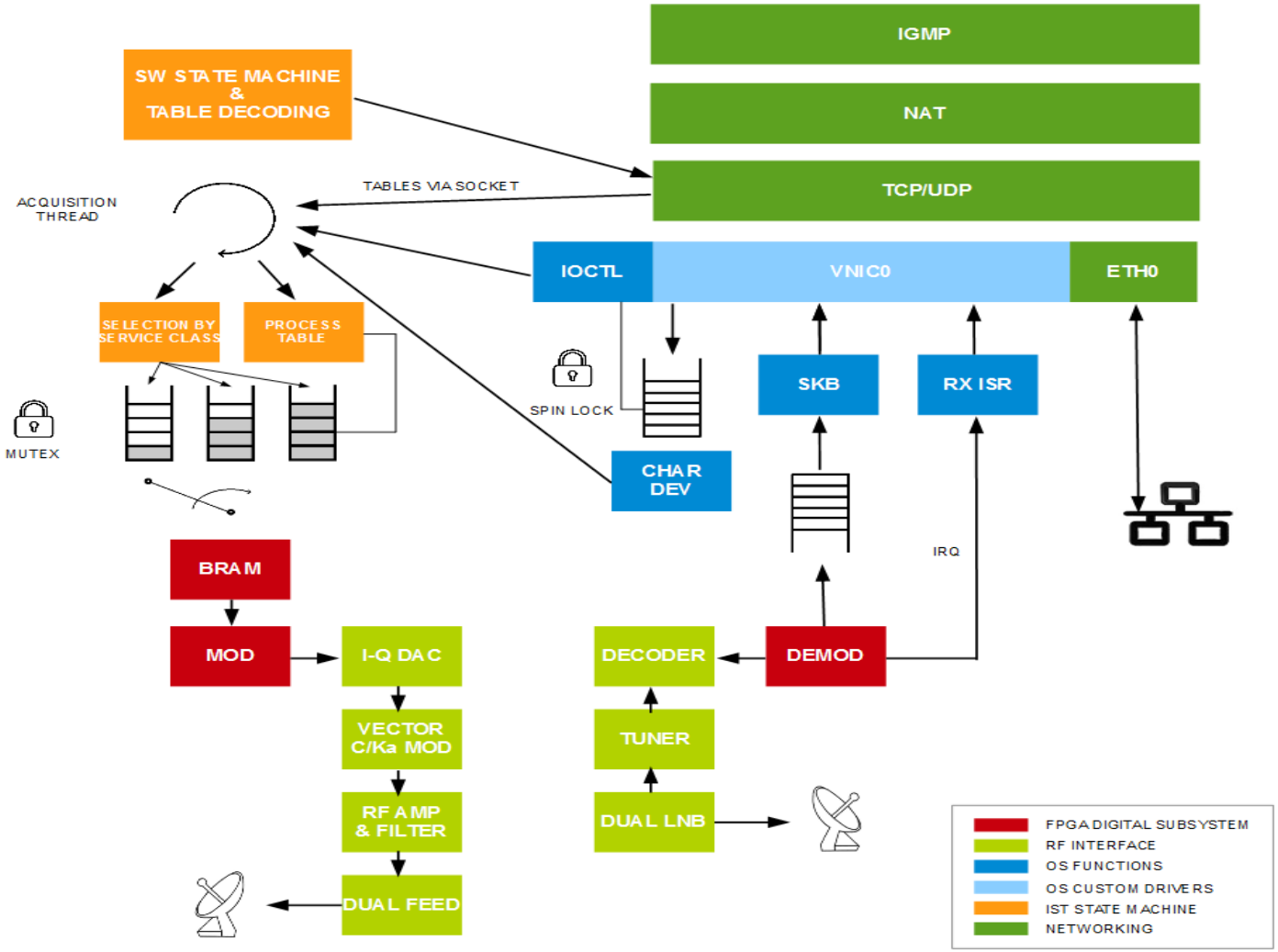
- ODU contains all main features
- FPGA full meet System Requir.
- Zynq 7020 is used
- Linux Debian Distribution
- Custom Logic Design
- HAN Modem
- ETH Re-built
- IPV4/IPV6
- Multi-use Coax Cable
- Double Tuner
- RF Filters
- DC Filters
- Low Phase Noise



Eutelsat Smart LNB- Satellite IP Modem-Router

Smart LNB Operating System

- Linux Debian Distribution
- Routing Input Queues
- IP Packetizing
- Priority Level Implement.
- MPE Decapsulation
- IP over DVB extracting
- Charge Device
- Socket Buffer
- NAT Manager
- IGMP
- DHCP Master/Slave
- Cold Logon
- Warm Logon
- Satellite Link Layer
- Quality of Service
- Satellite Link Manager



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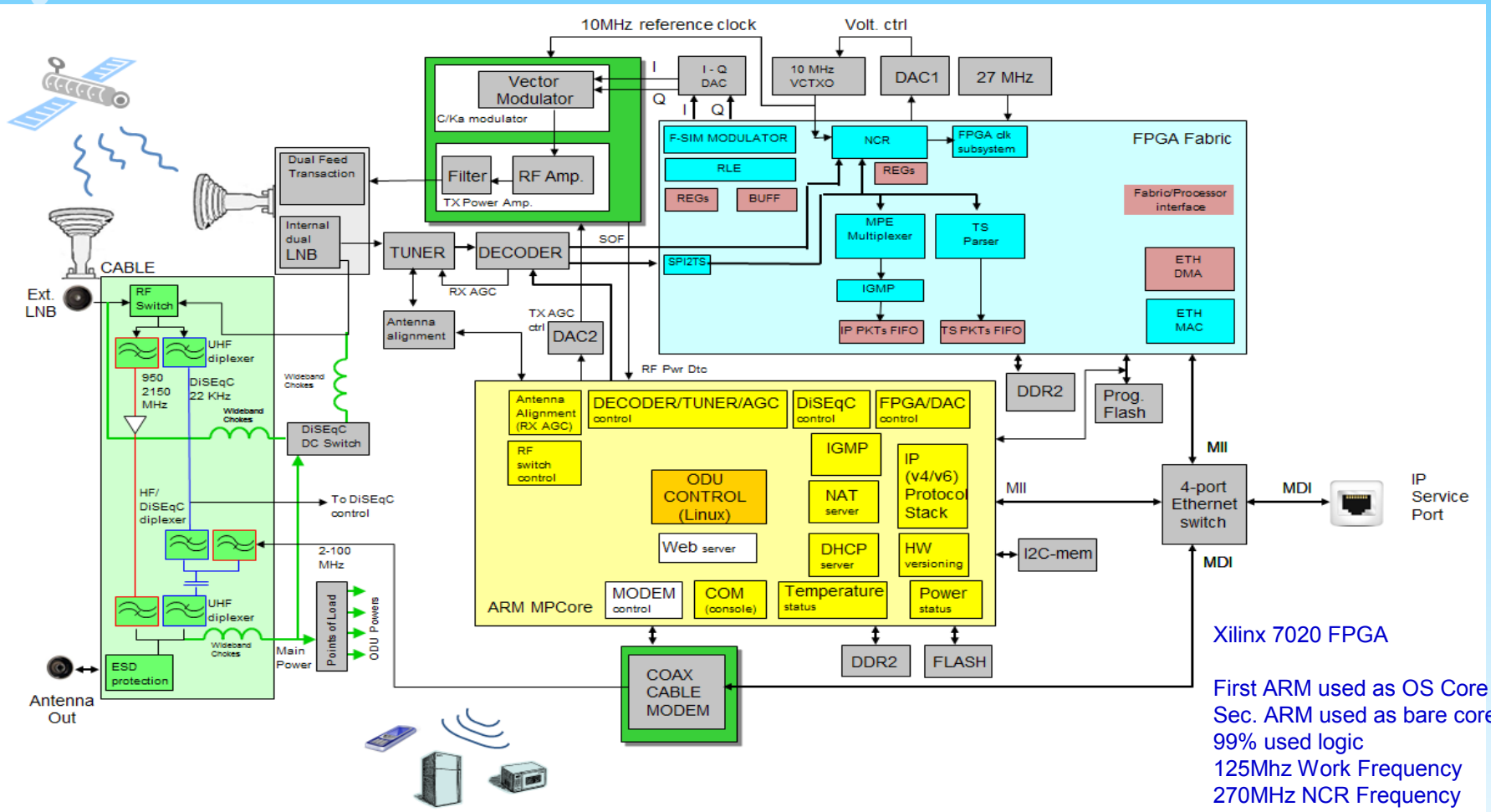
Eutelsat Smart LNB- Satellite IP Modem-Router

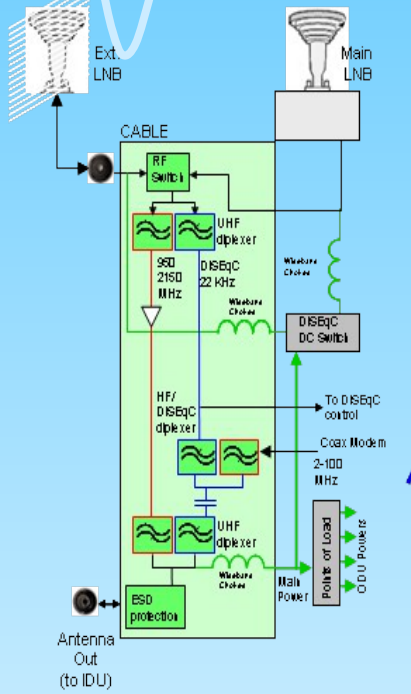


Xilinx 7020 FPGA

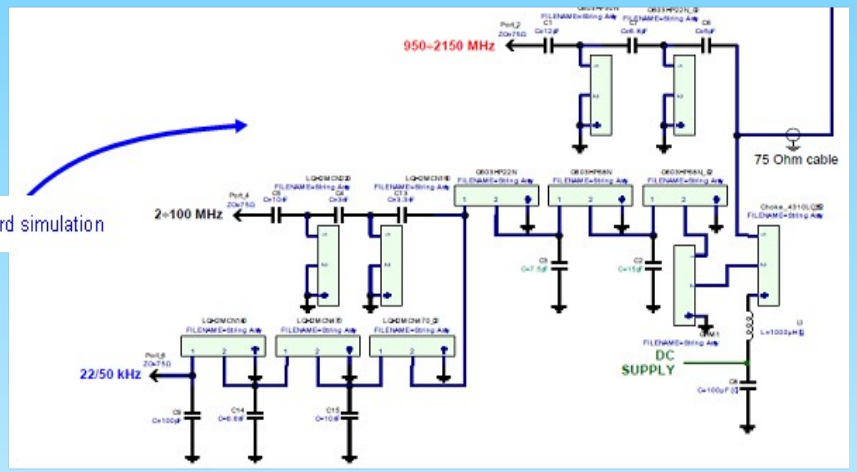
First ARM used as OS Core
Sec. ARM used as bare core
99% used logic
125Mhz Work Frequency
270MHz NCR Frequency

MindWay
Power to make

Eutelsat Smart LNB- Satellite IP Modem-Router

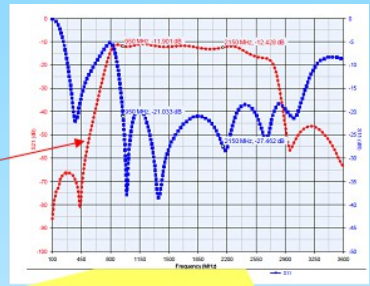


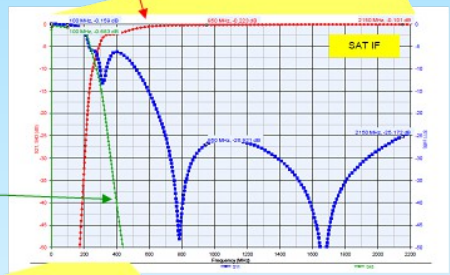
Filter card simulation



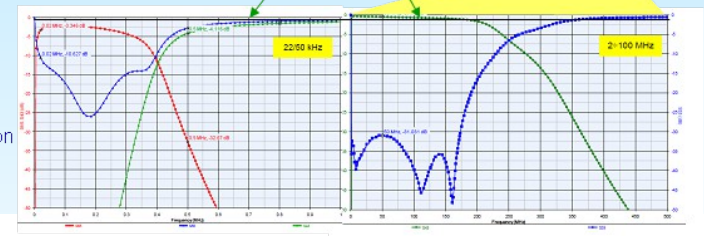
Simulation model

SAT IF (red)





Coax modem (green)



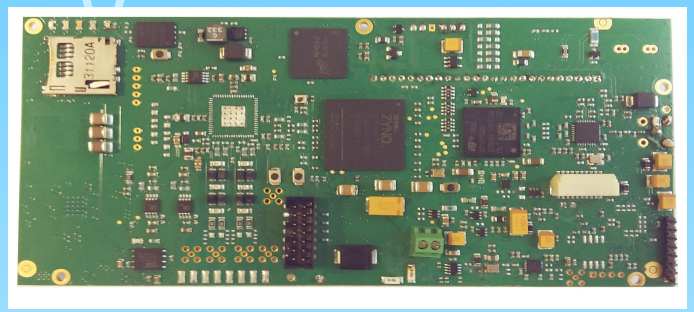
Coax Cable Simulation

Cable Filtering Design

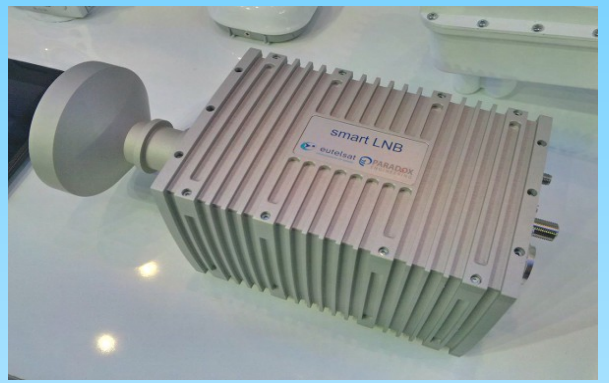
- All bands allocated in one coax cable
- DC band
- Service Band
- HAN Modem Band
- IF Band
- RF Band

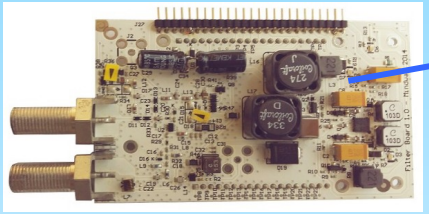
MindWay
Power to make

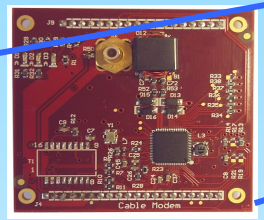
FPGA Centric System Design Methodology



- ODU Motherboard with Zynq (Mindway Design)

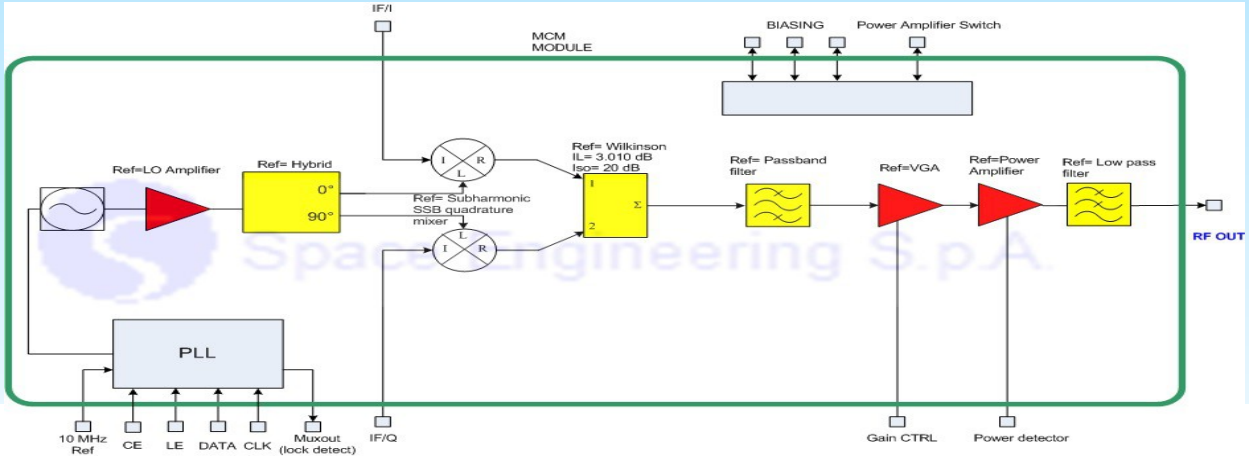






- Filter & Cable Modem Boards (Mindway Design)

- RF Module (third party implementation)



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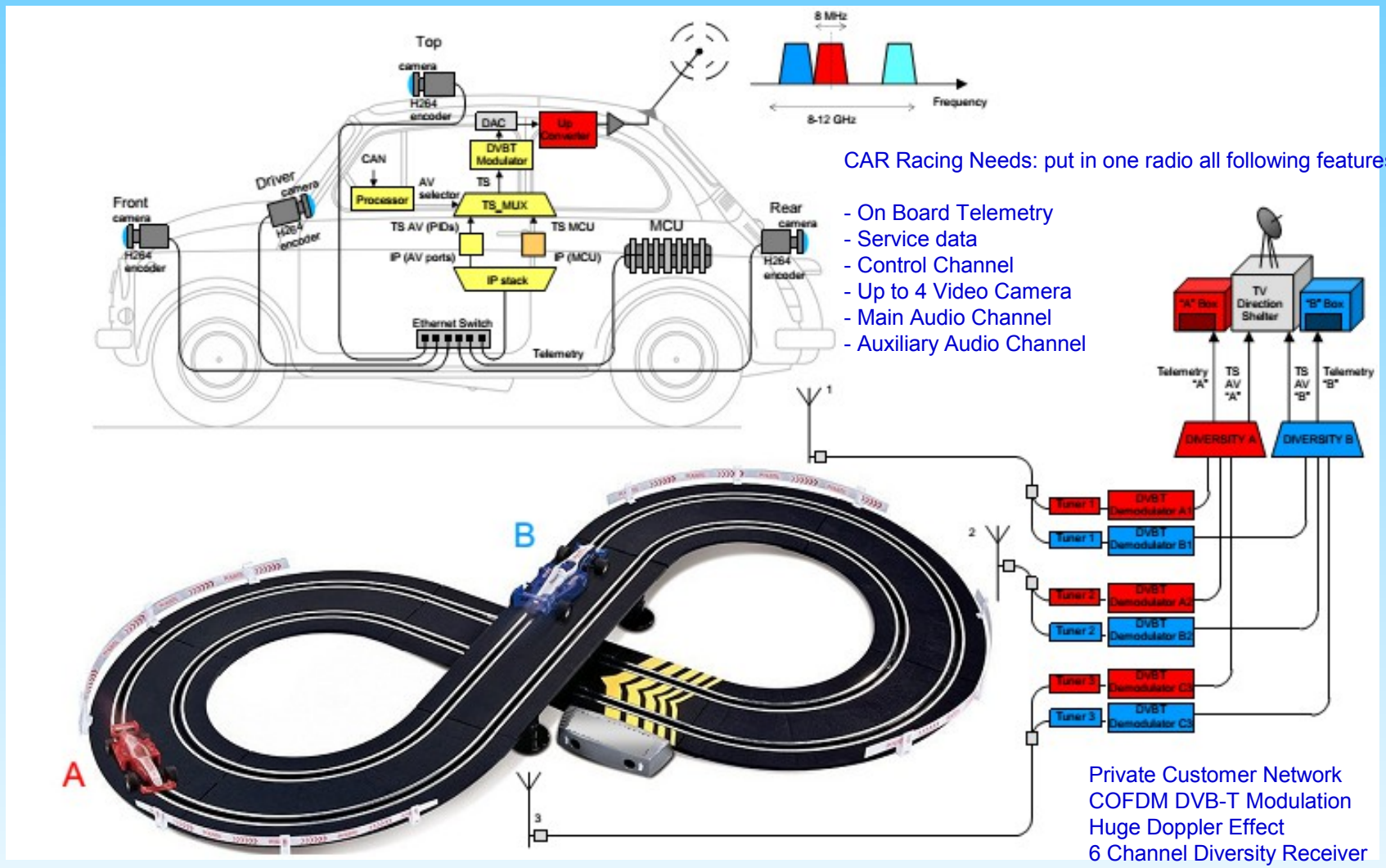
Power to make

Car Racing Audio-Video-Telemetry CAR System



MindWay
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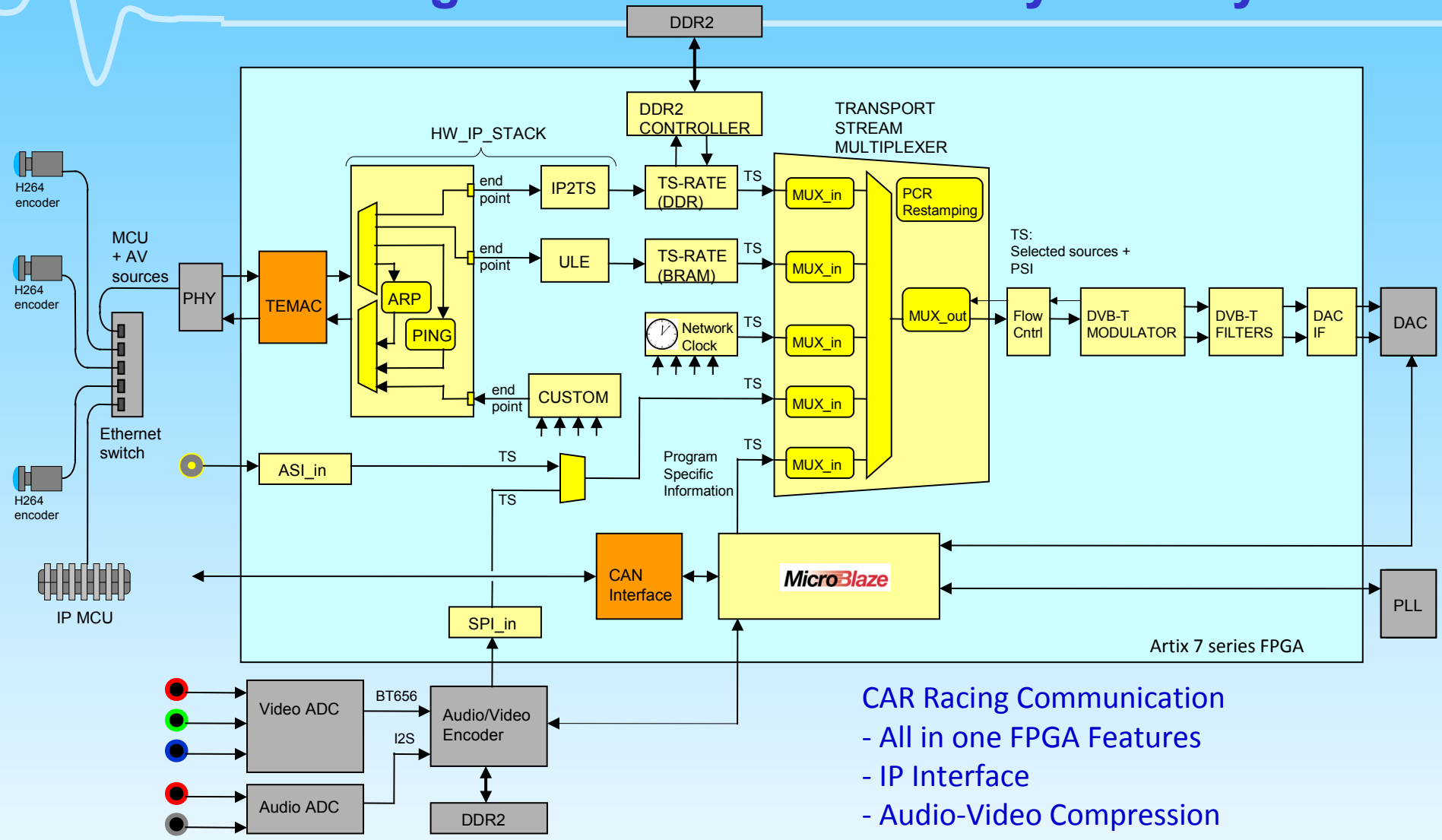
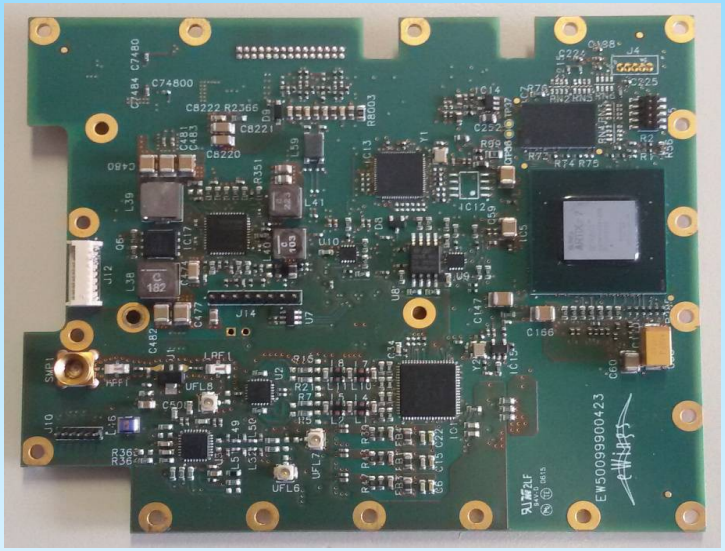
F1 Car Racing Audio-Video-Telemetry CAR System



CAR Racing Communication
- All in one FPGA Features
- IP Interface
- Audio-Video Compression
- TS Multiplexer
- DVB-T Modulation

MindWay
Power to make

Car Racing Audio-Video-Telemetry CAR System



Car Racing on-Car Remote Telemetry

- Xilinx Artix 200, Embedded Microblaze Microctrl
- DDR2 1 Gbyte RAM
- 4 ASI / IP Input
- Up to 4 High Definition TS Audio / Video Streams
- TS / IP Audio/Video Demultiplexer – Multiplexer
- Video and Audio over IP Trasport
- ULE Encapsulator
- CAN Command Interface
- Serial Interface and Monitoring
- DVB-T Standard Modulator
- RF and Power management

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Power to make