

Highly Reliable System-on-Chip using Dynamical Reconfigurable FPGAs

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Goal

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- Analysis of Single Event Upset sensitivity of SRAM-based FPGAs
 - Identification of Single Points of Failure (SPFs)
 - Error rate estimation
- Mitigation

Outline

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- Introduction: SEU scenario
- Verification and Error Rate Integrated tool (VERI-Place)
 - Configuration memory Database
 - Execution flow
 - Results and Classification
- Experimental results
 - Radiation test and Fault Injection
- Conclusions and future works

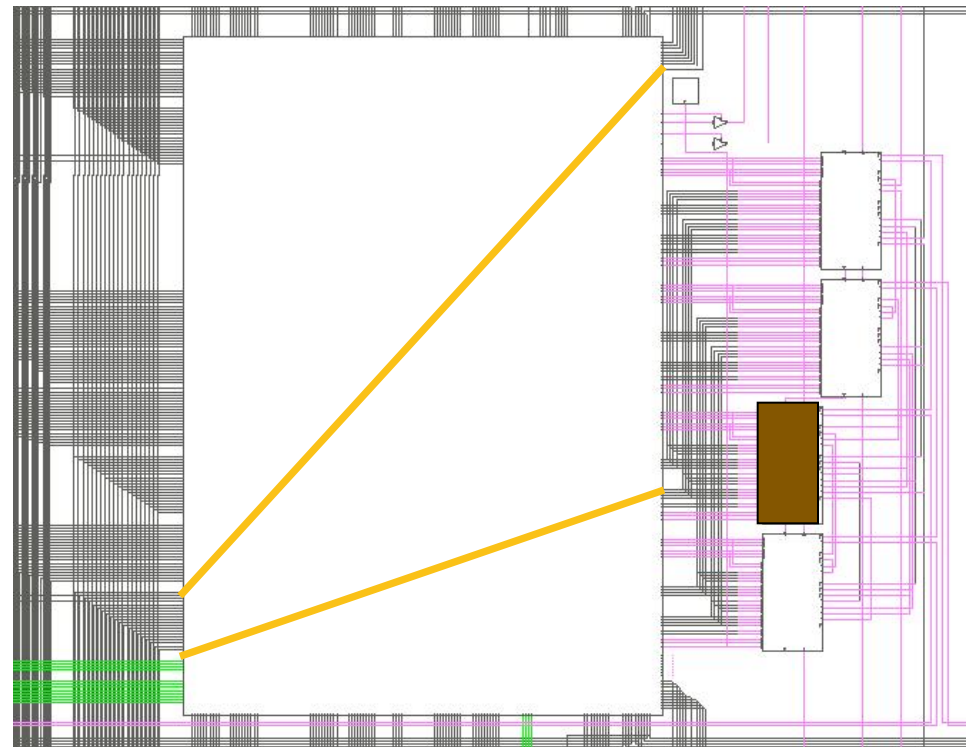
SEU scenario

4

- The bitstream

0	1	0	0	0	0
1	0	0	0	0	0
1	1	0	0	0	0
0	0	0	0	1	0
0	1	0	1	0	0
0	0	0	0	0	0

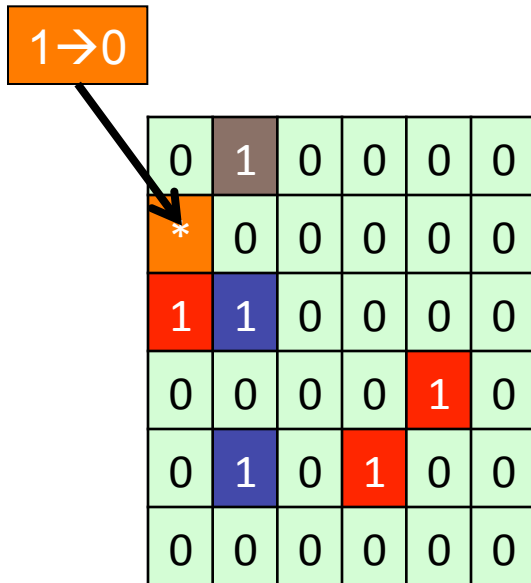
- The original netlist



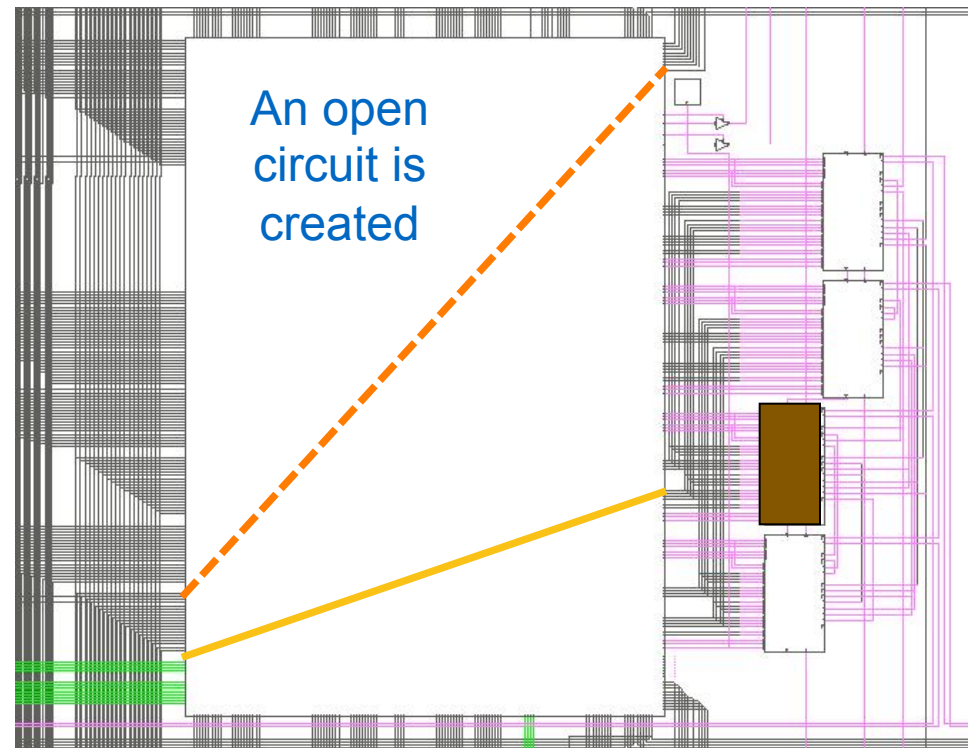
SEU scenario

5

□ The bitstream



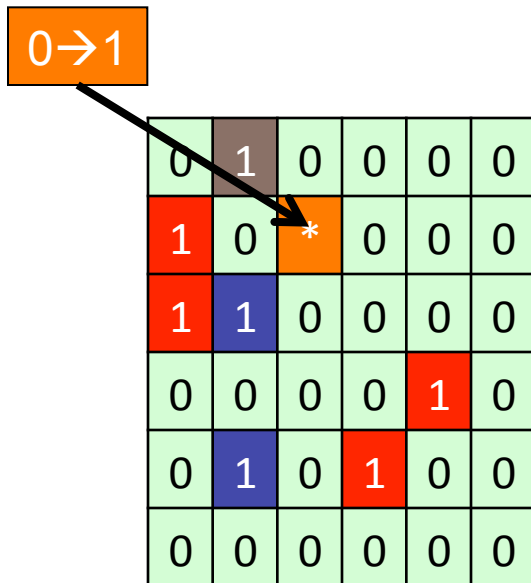
□ The corrupted netlist



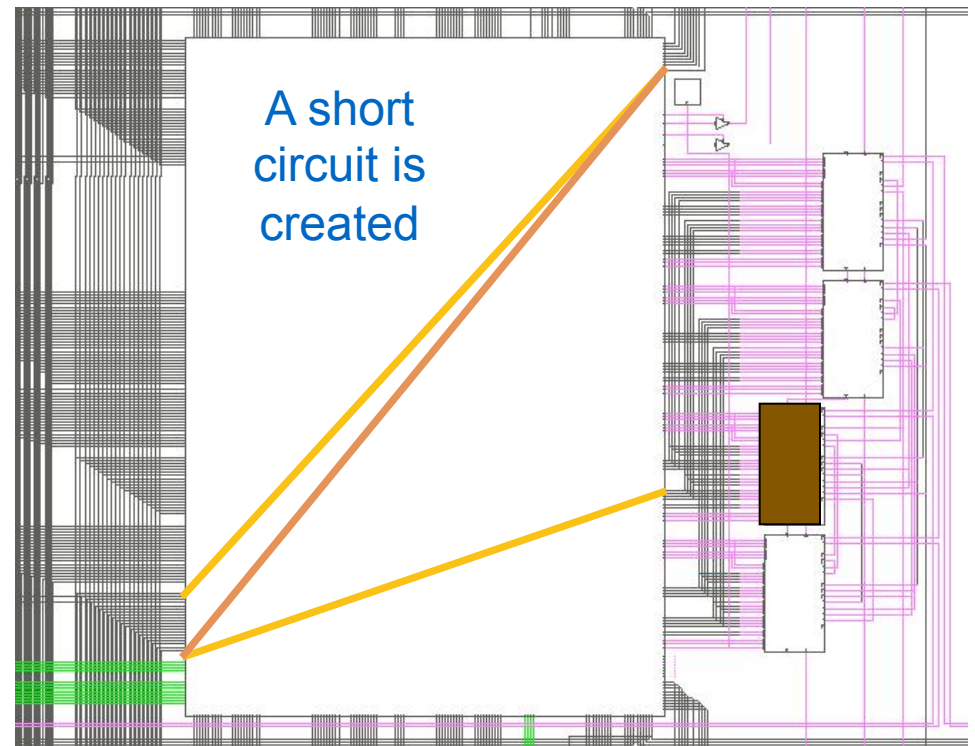
SEU scenario

6

□ The bitstream



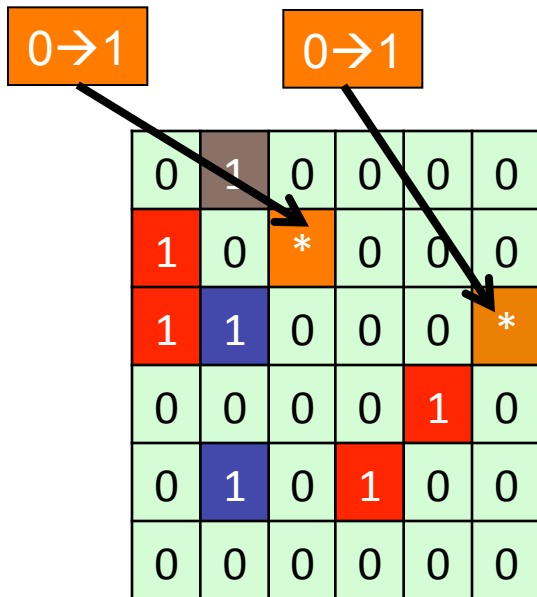
□ The corrupted netlist



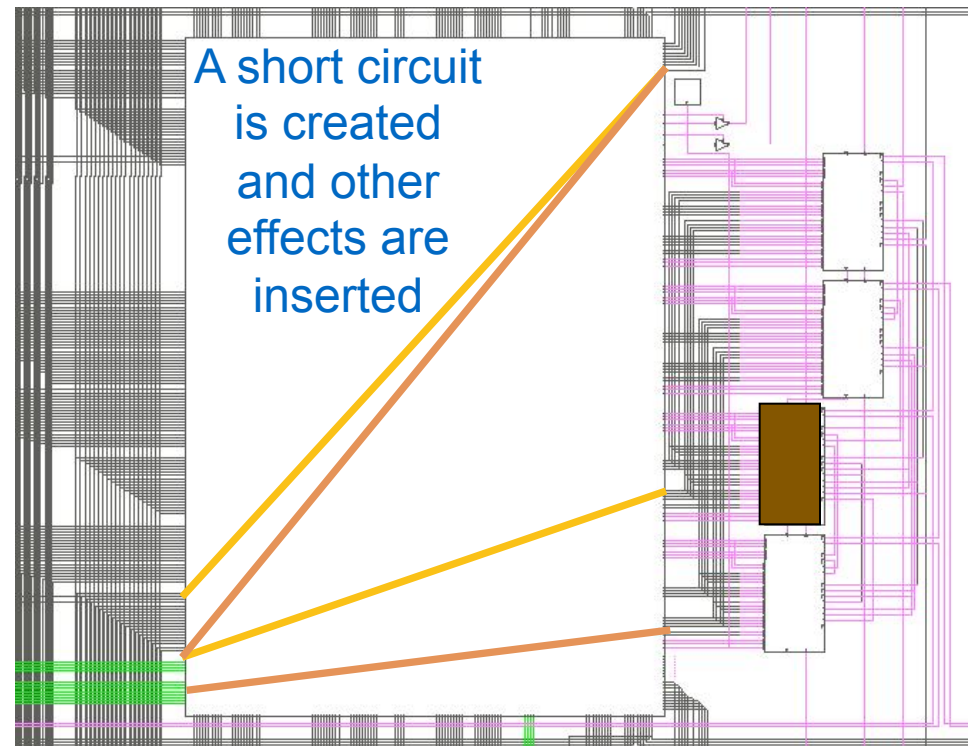
SEU scenario: accumulation of 2-bit

7

□ The bitstream



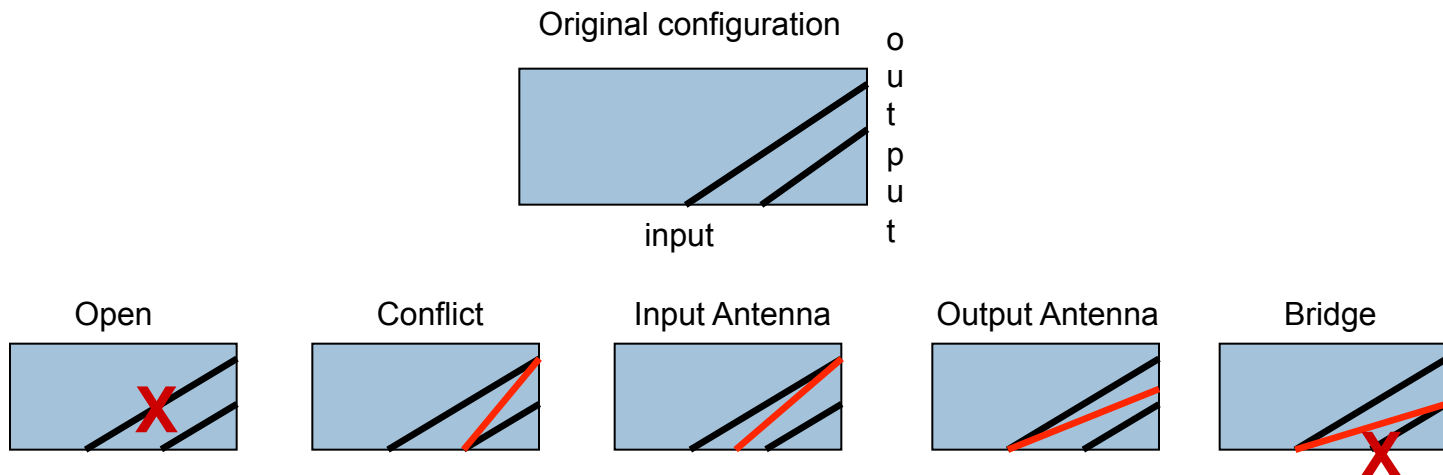
□ The corrupted netlist



SEU scenario

8

- SEU within the configuration memory
 - FPGA resource not affected : **NO ERROR**
 - FPGA resource affected : **ERROR**
- SEU induced architectural modification
 - **Logic Element: LUT, MUX, FF Config**
 - **Interconnections: Switchbox**

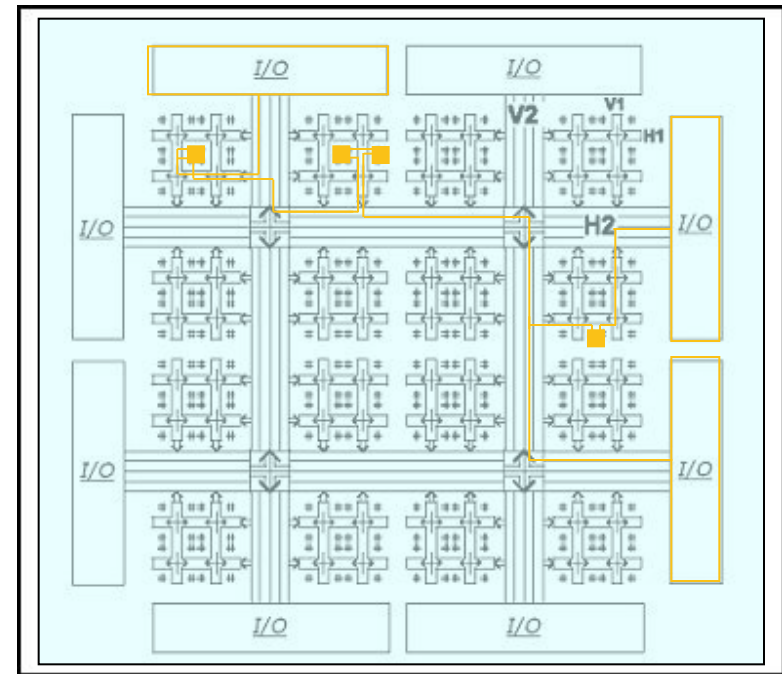


SEU scenario

9

0	1	0	0	0	0
1	0	0	0	0	0
1	1	0	0	0	0
0	0	0	0	1	0
0	1	0	1	0	0
0	0	0	0	0	0

FPGA configuration
memory



FPGA array

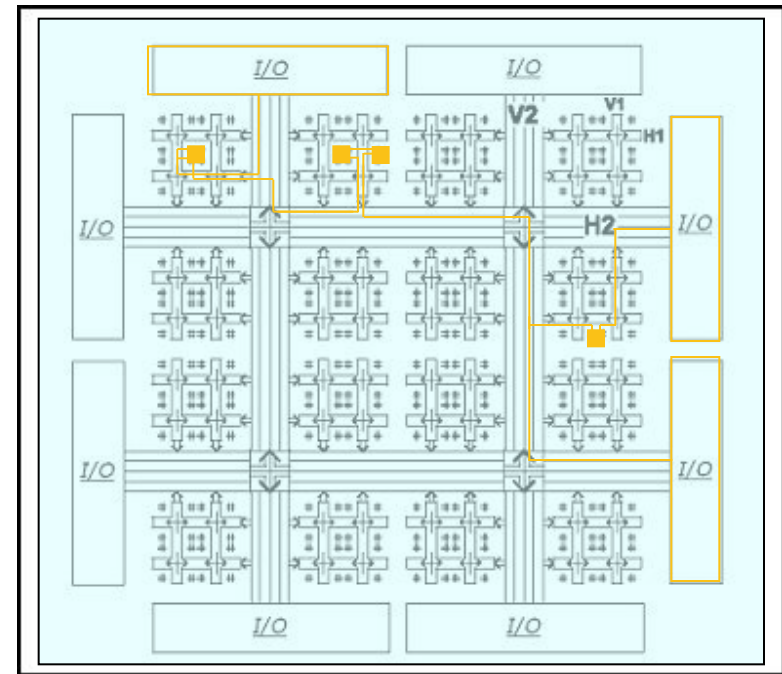
Execution time

SEU scenario

10

0	1	0	0	0	0
1	0	0	0	0	0
1	1	0	0	0	0
0	0	0	0	1	0
0	1	0	1	0	0
0	0	0	0	0	0

FPGA configuration
memory



FPGA array

Execution time

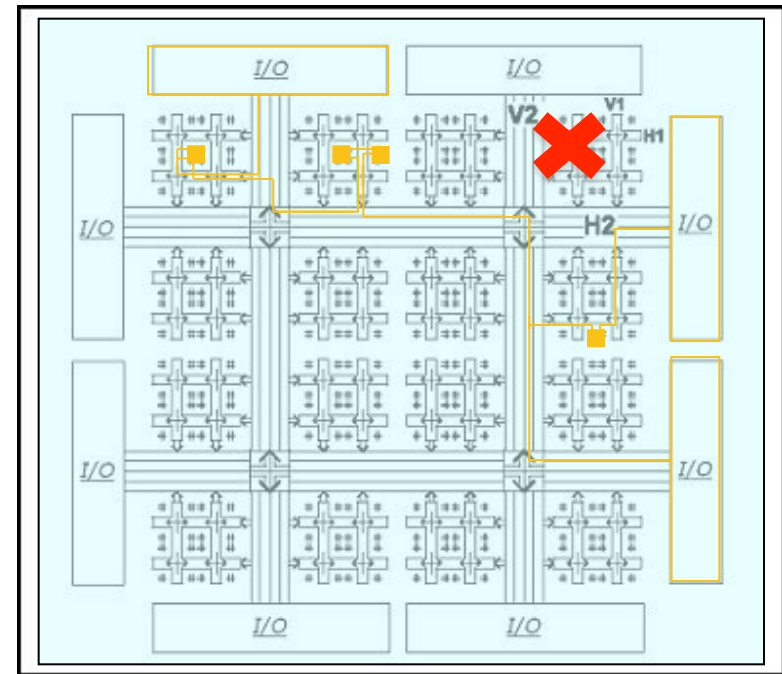


SEU scenario

11

0	1	0	0	0	0
1	0	0	0	0	0
1	1	0	0	0	0
0	0	0	0	1	0
0	1	0	1	0	0
0	0	0	0	0	0

FPGA configuration
memory



FPGA array

Execution time

SEU effect

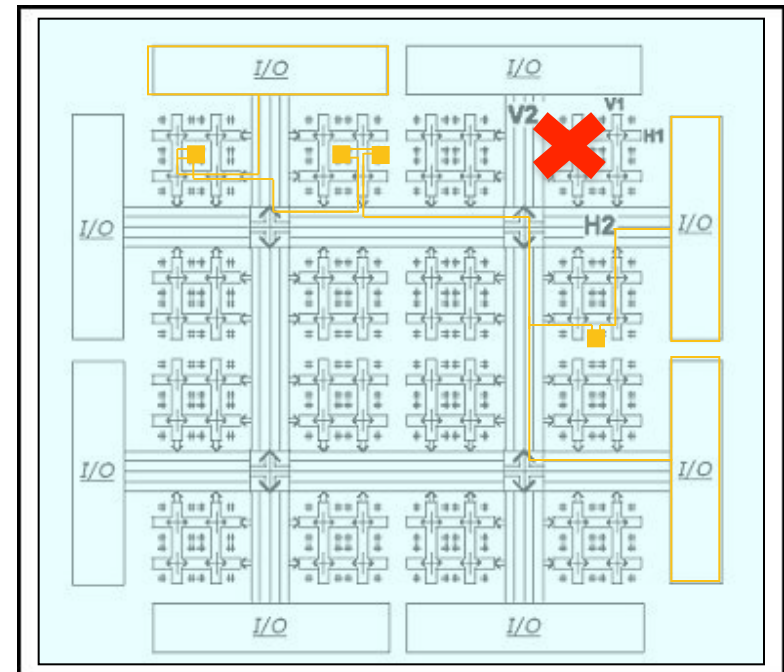


SEU scenario

12

0	1	0	0	0	0
1	0	0	0	0	0
1	1	0	0	0	0
0	0	0	0	1	0
0	1	0	1	0	0
0	0	0	0	0	0

FPGA configuration
memory



FPGA array

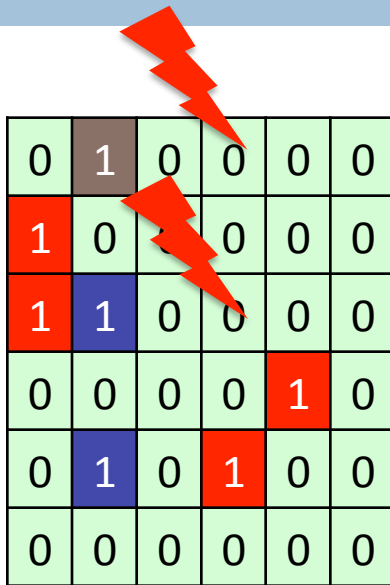
SEU effect: No error



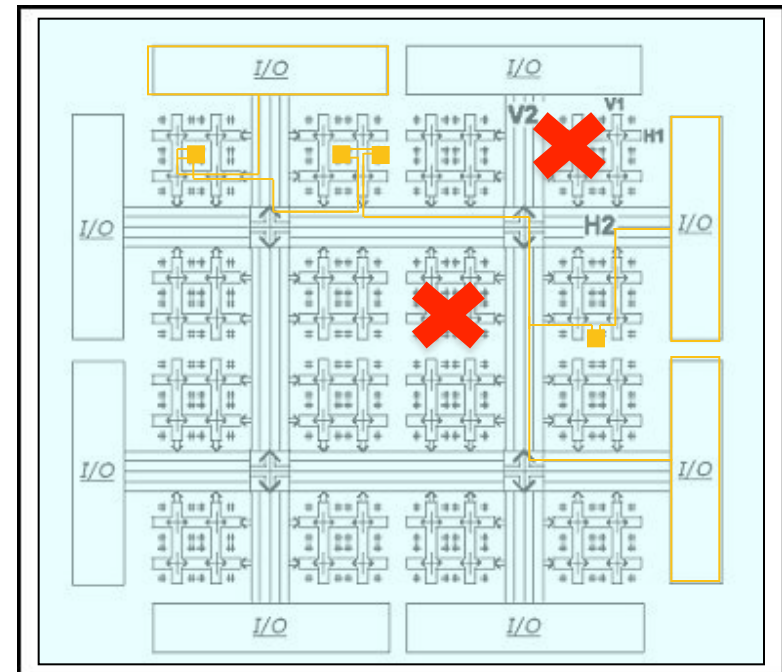
Execution time

SEU scenario

13



FPGA configuration
memory



FPGA array

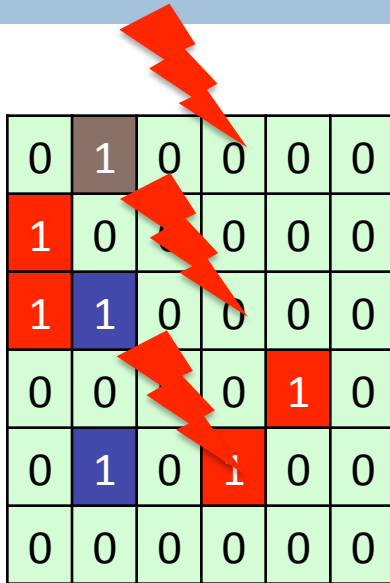
Execution time

SEU effect: No error

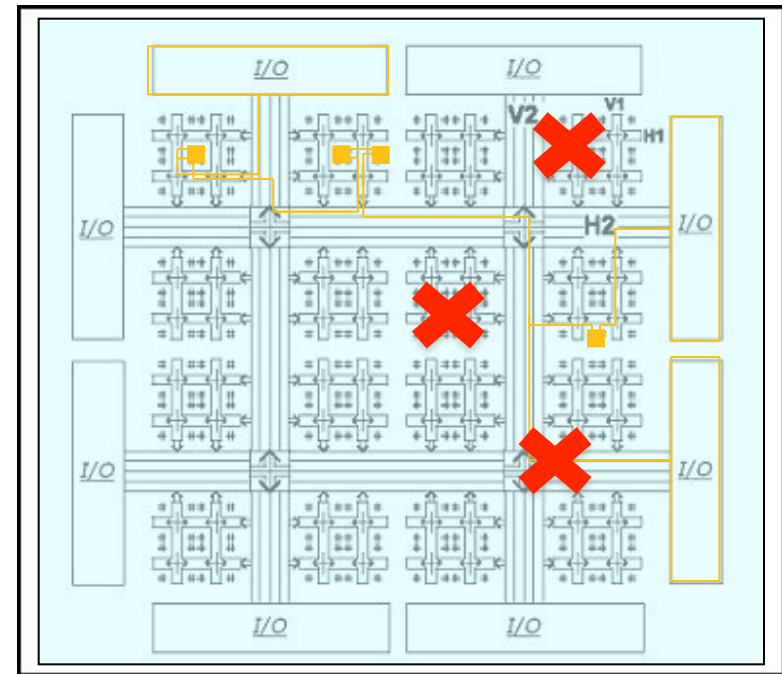


SEU scenario

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FPGA configuration
memory



FPGA array

Execution time

SEU effect: No error

SEU effect: Error

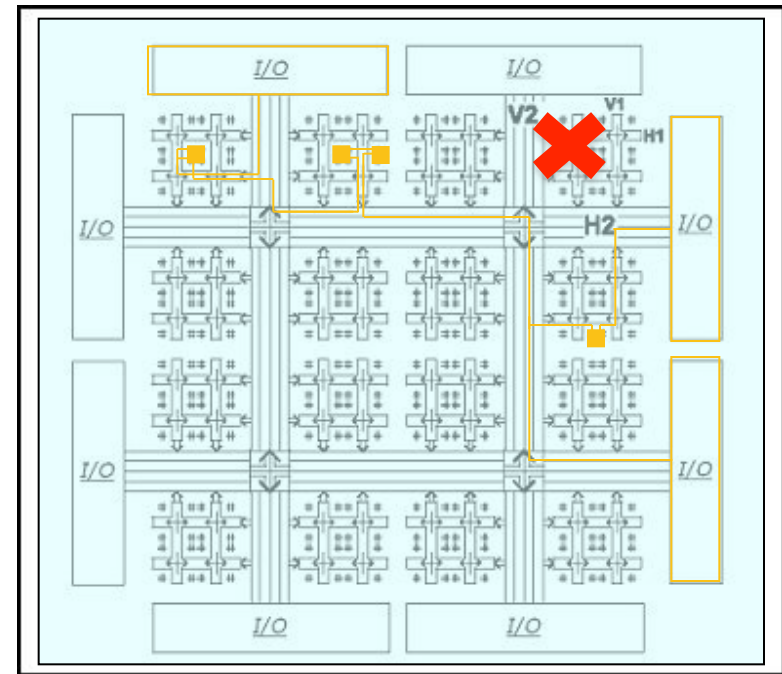


SEU scenario with scrubbing

15

0	1	0	0	0	0
1	0	0	0	0	0
1	1	0	0	0	0
0	0	0	0	1	0
0	1	0	1	0	0
0	0	0	0	0	0

FPGA configuration
memory



FPGA array

Execution time SEU effect

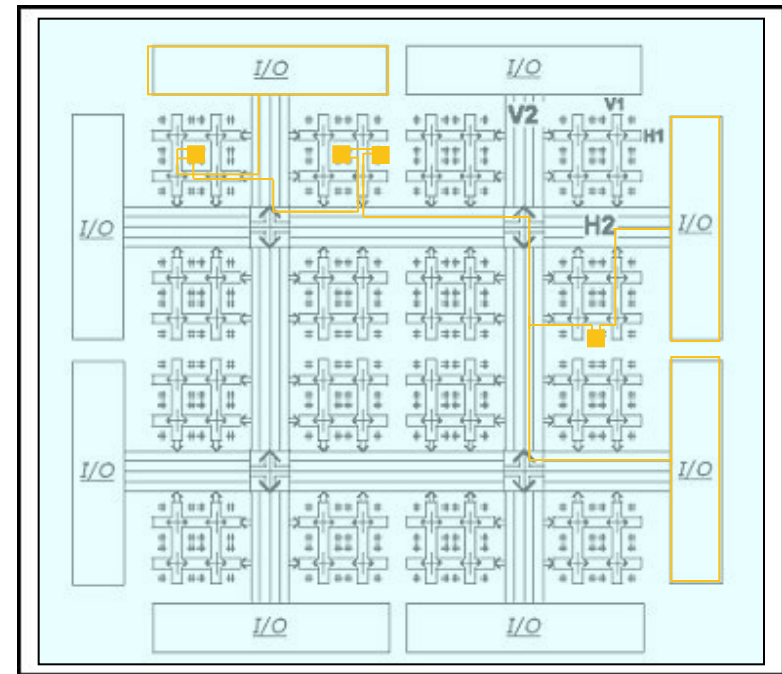


SEU scenario with scrubbing

16

0	1	0	0	0	0
1	0	0	0	0	0
1	1	0	0	0	0
0	0	0	0	1	0
0	1	0	1	0	0
0	0	0	0	0	0

FPGA configuration
memory



FPGA array

Execution time SEU effect Scrub cycle

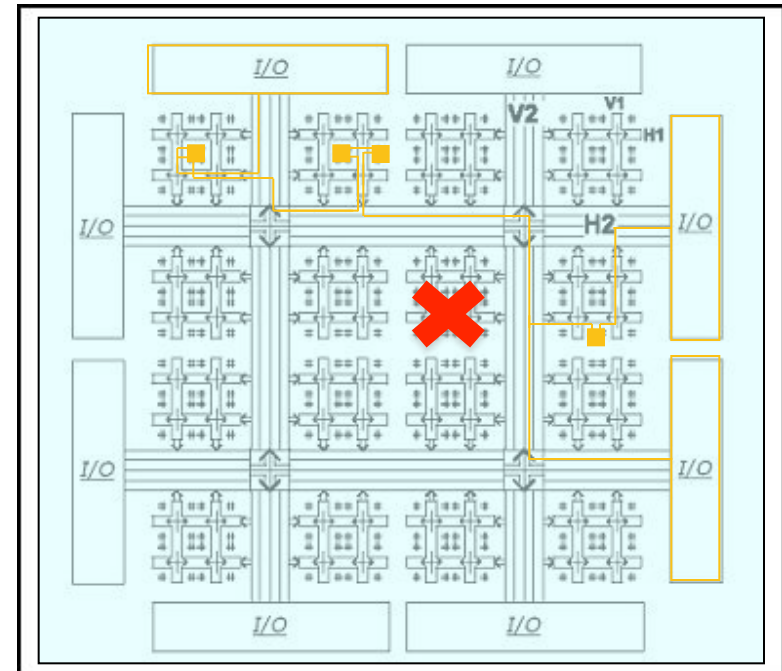


SEU scenario with scrubbing

17

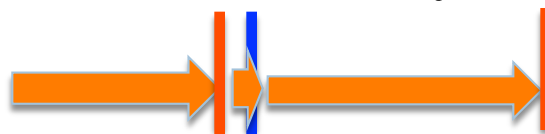
0	1	0	0	0	0
1	0	0	0	0	0
1	1	0	0	0	0
0	0	0	0	1	0
0	1	0	1	0	0
0	0	0	0	0	0

FPGA configuration
memory



FPGA array

Execution time SEU effect Scrub cycle

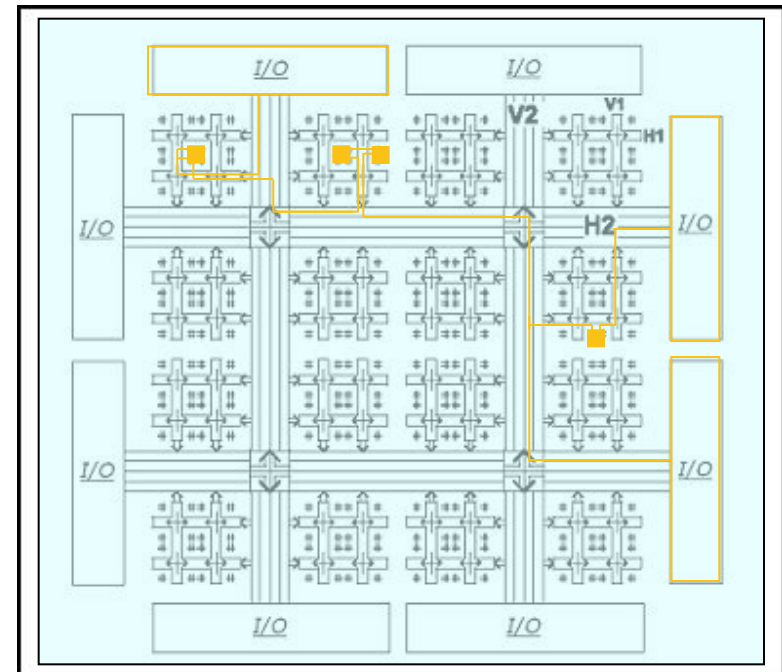


SEU scenario with scrubbing

18

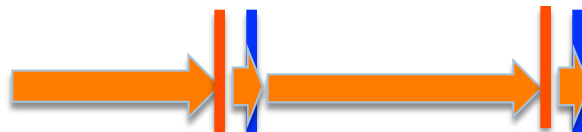
0	1	0	0	0	0
1	0	0	0	0	0
1	1	0	0	0	0
0	0	0	0	1	0
0	1	0	1	0	0
0	0	0	0	0	0

FPGA configuration
memory



FPGA array

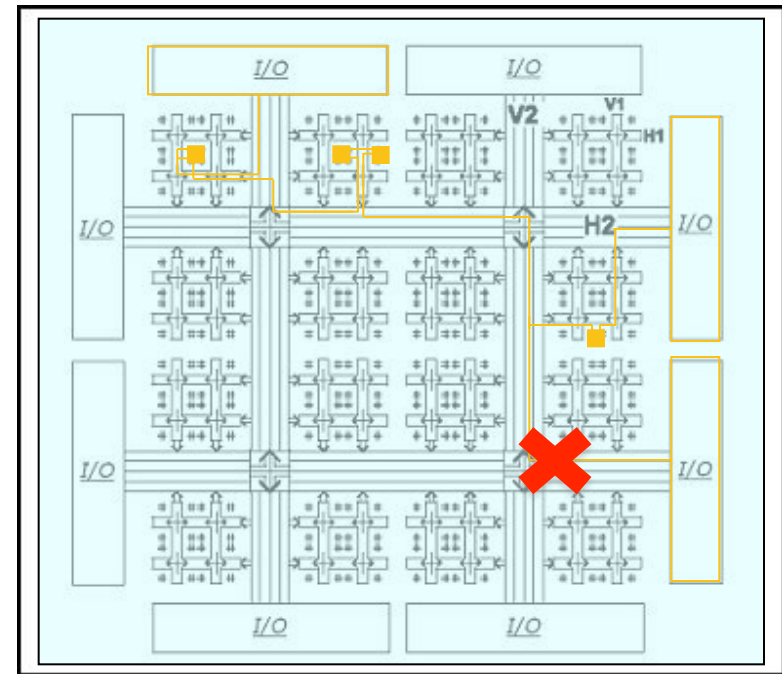
Execution time SEU effect Scrub cycle



SEU scenario with scrubbing

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0	1	0	0	0	0
1	0	0	0	0	0
1	1	0	0	0	0
0	0	0	0	1	0
0	1	0	1	0	0
0	0	0	0	0	0



FPGA configuration memory

FPGA array

Execution time SEU effect Scrub cycle

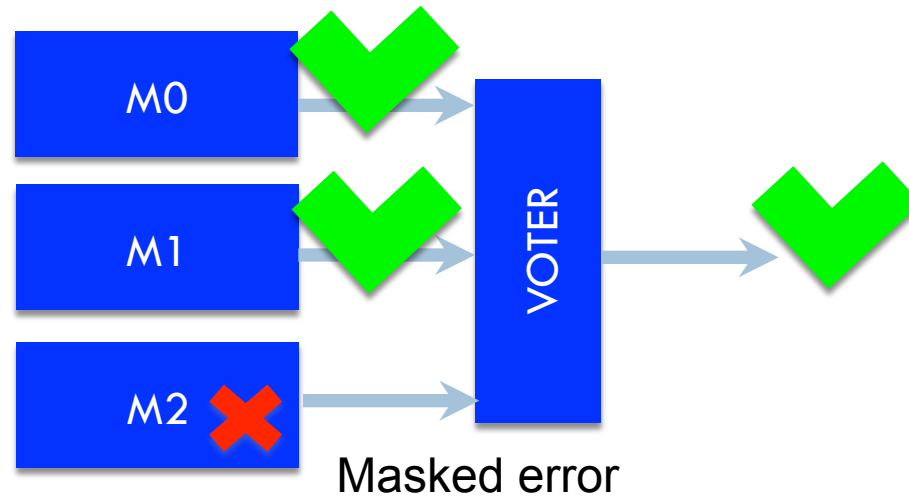
SEU effect: Error



SEU scenario

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TMR

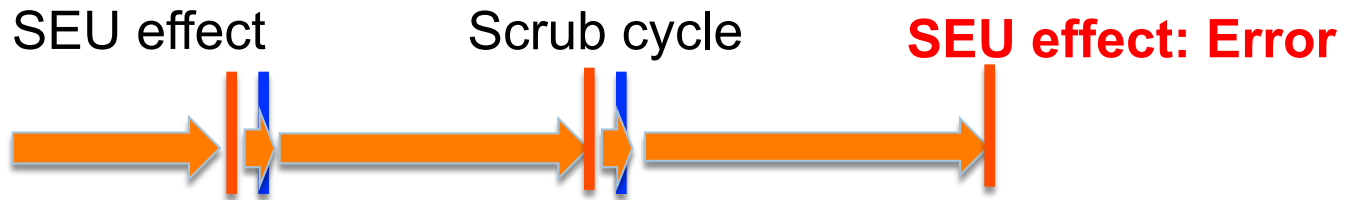


- The application of Netlist-based TMR and scrubbing is an effective solution
 - ▣ Drawbacks: power consumption and functional availability

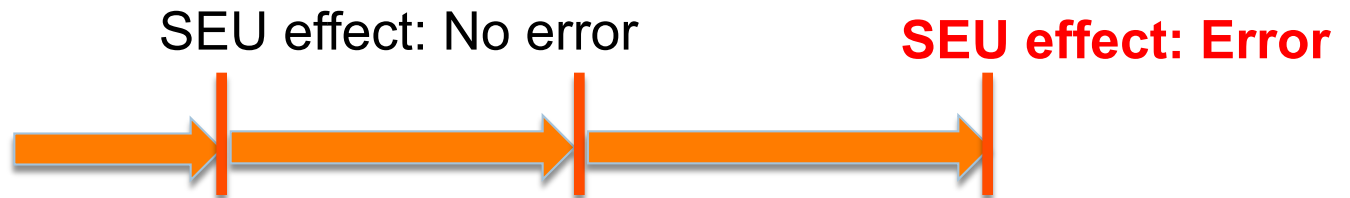
SEU scenario

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**with
scrubbing**

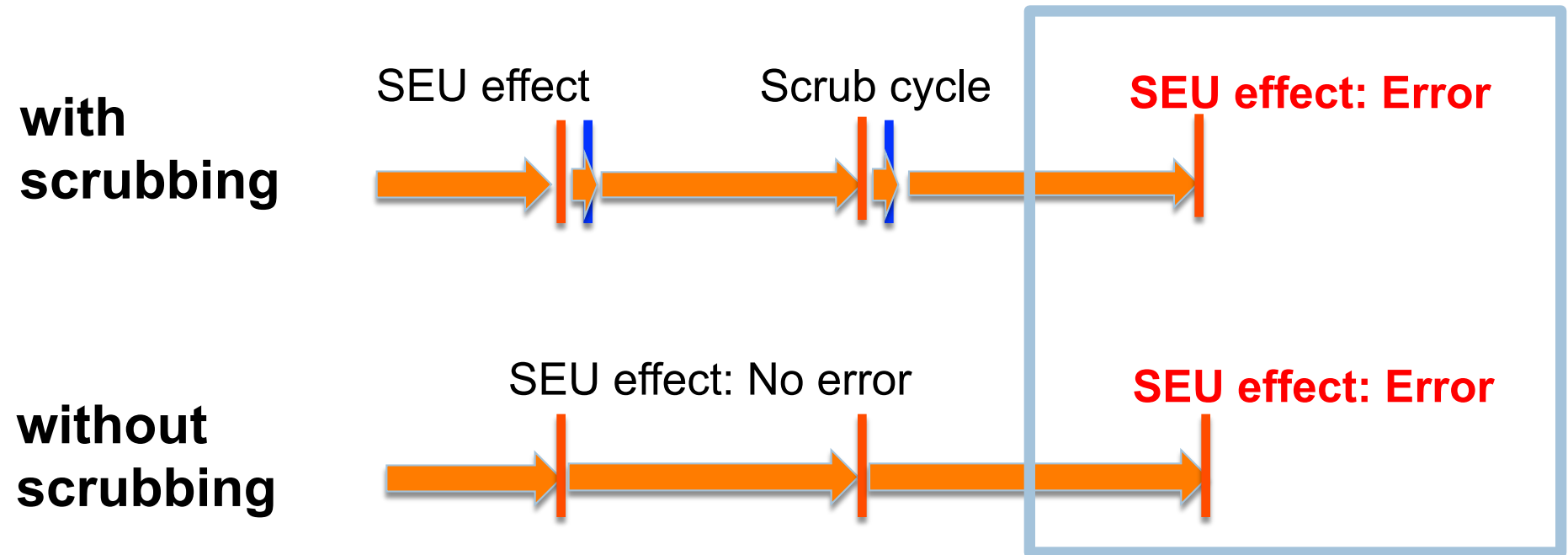


**without
scrubbing**



SEU scenario

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Errors affecting the circuit outputs happen at the same time

- **Probability of SEU location**
- Avoid of SPFs: **TMR is a MUST**

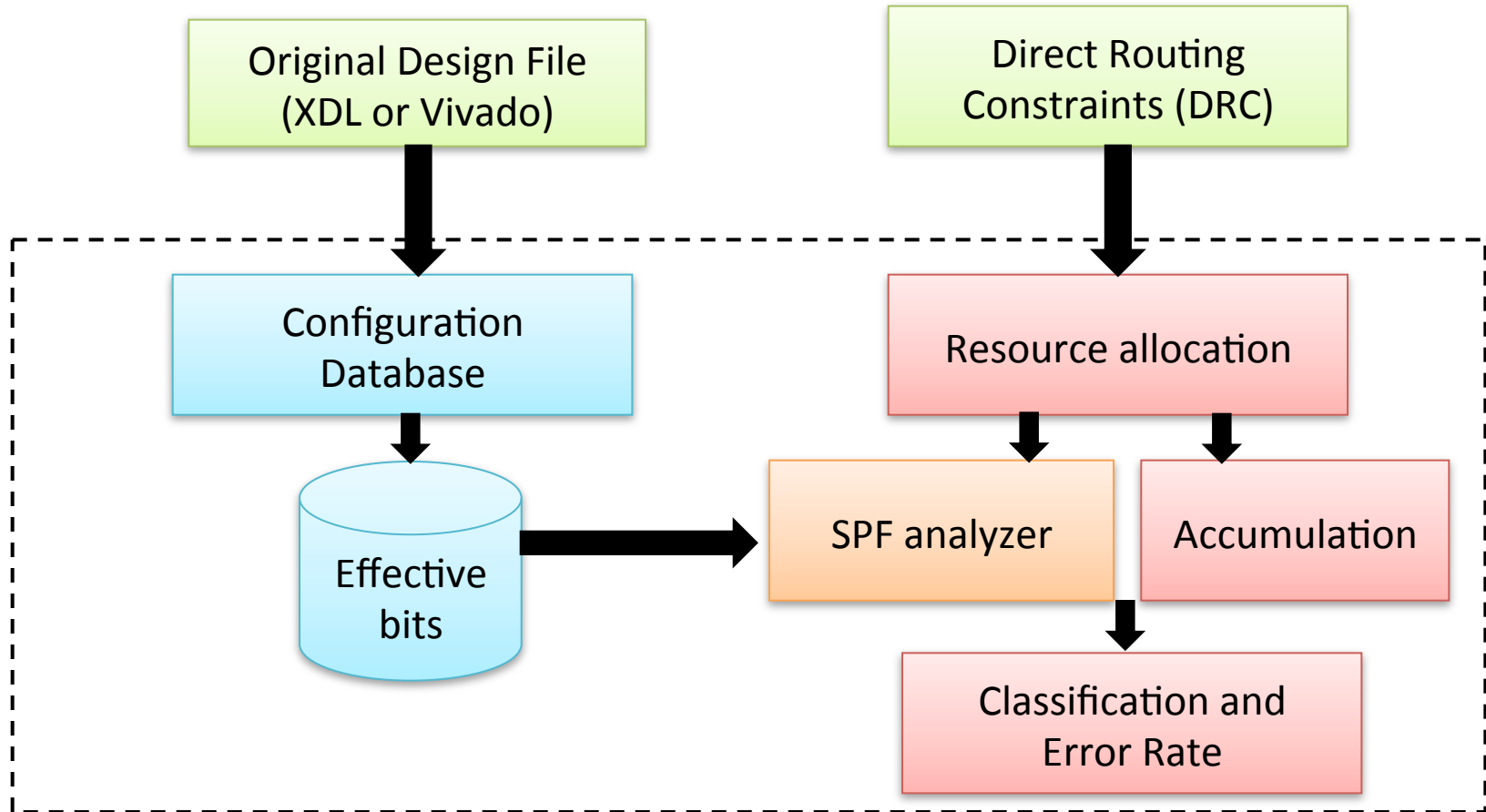
The proposal: VERI-Place tool

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- Measurement of the Application Error Probability (AEP)
 - Number of SEUs in the FPGAs configuration memory until an output error is observed
- Analysis of different design techniques
 - Fault tolerance (DWC, TMR, XTMR,...)
 - Static
 - Dynamic
 - Partial and dynamic

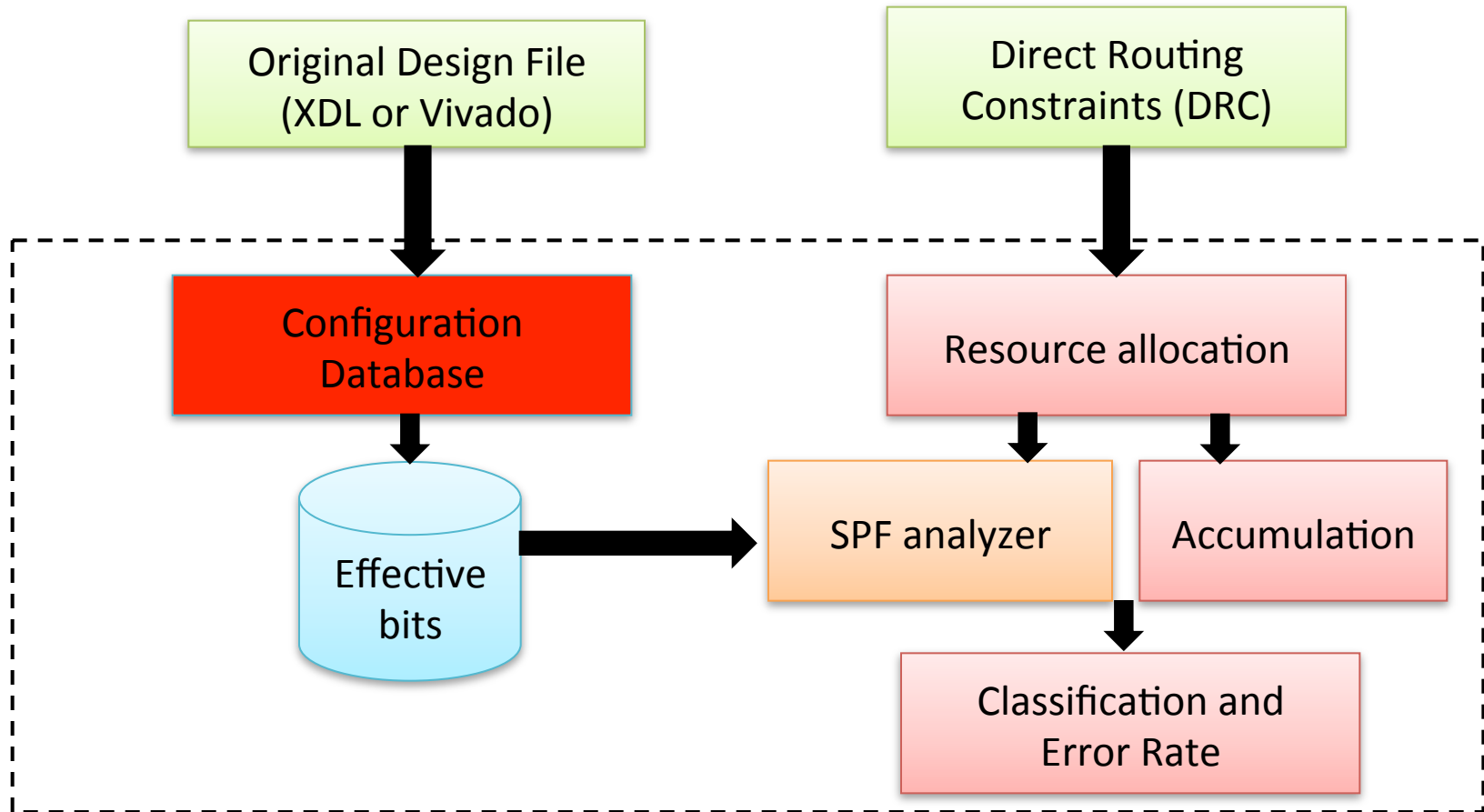
The proposal: VERI-Place tool

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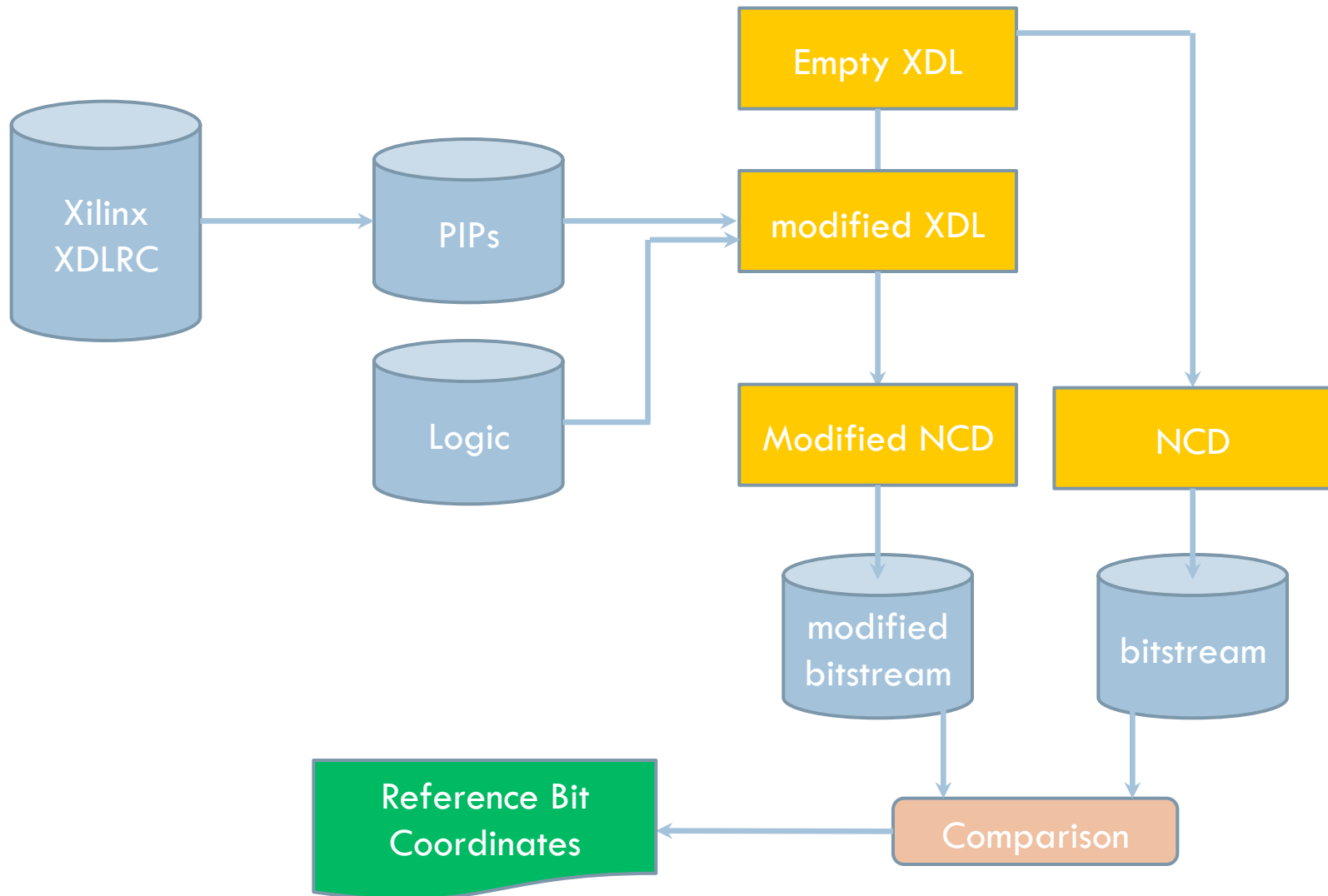
The proposal: VERI-Place tool

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Configuration memory DB

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Configuration memory DB

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Device Name	Total PIP [#]	Effective PIP [#]
XC5VLX50T-FF1136	18,975,457	15,695
XC7K70E-2FBG676	29,466,958	21,081
XC7K325T-2FBG900	123,919,224	21,081

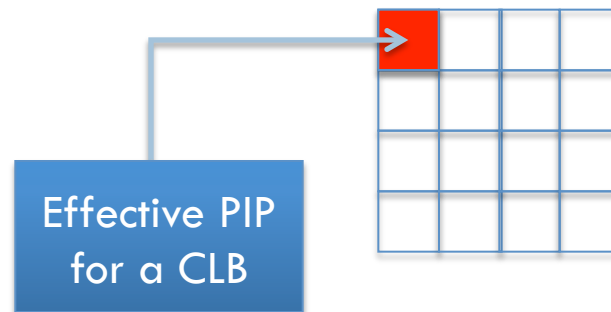
- PIPs of the whole FPGA architecture
- PIPs replica are on different CLB positions
- A PIP requires about 30-35 seconds to be decoded
 - ▣ **XC7K70E would require about 32 years!**
- FPGA array is regular, apart from *specific* architectural PIPs
 - ▣ unique PIPs of a given FPGA device are distinguishable

Configuration memory DB

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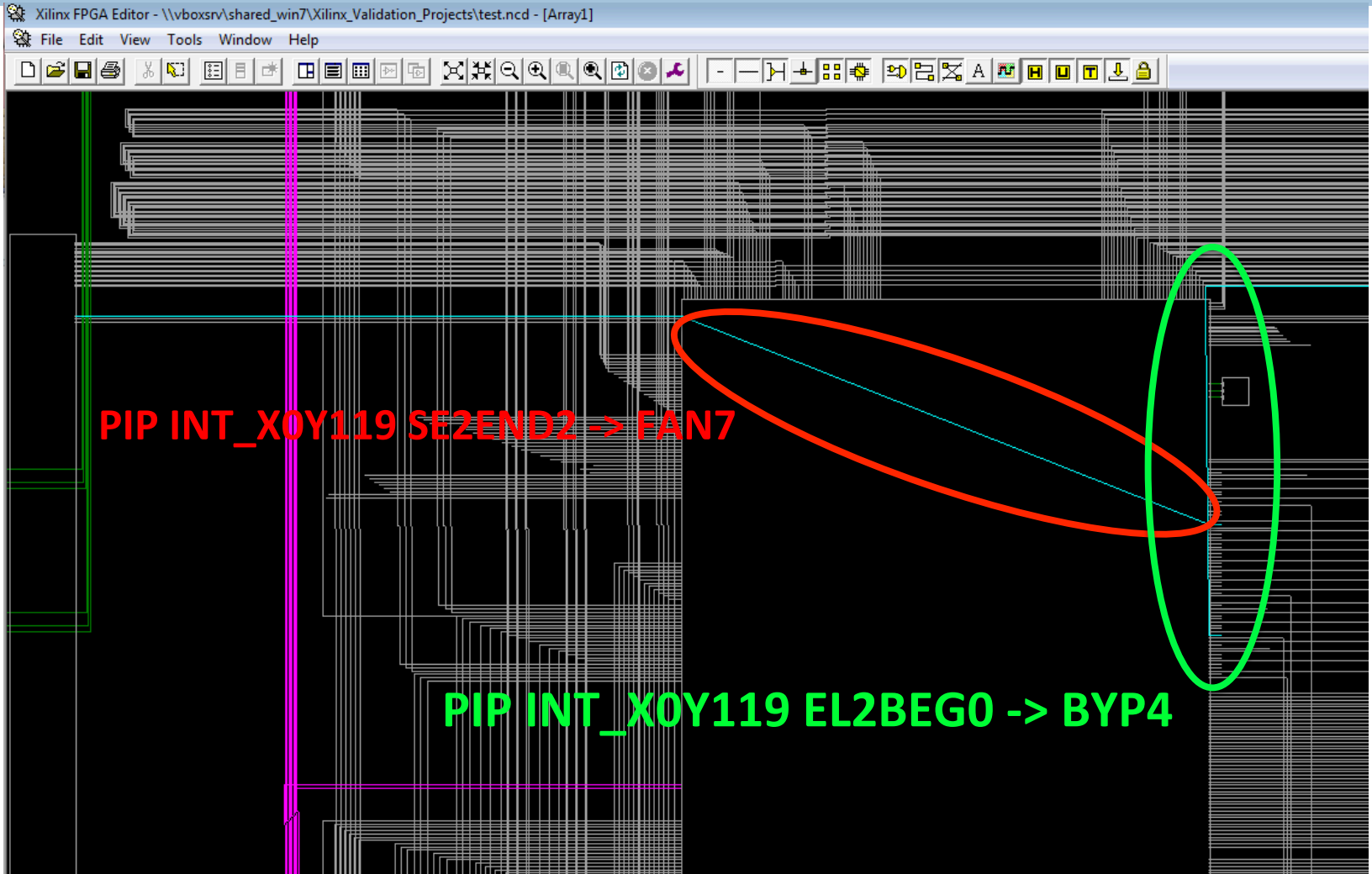
Device Name	Effective PIPs [#]	Decoding [days]
XC5VLX50T-FF1136	15,695	≈6.5
XC7K70E-2FBG676	21,081	≈8.6
XC7K325T-2FBG900	21,081	≈12.3

- The decoding is performed on effective PIPs
- The whole PIP coding is generated calculating the configuration memory offset between different CLBs



Real Coding Xilinx Virtex-5LX50T

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Real Coding Xilinx Virtex-5LX50T

30

- PIP INT_XOY119 SE2END2 -> FAN7

3.693.213

3.693.214

3.693.831

3.693.835

4 configuration memory bits.

In order to have the PIP these bits must be fixed at logic value '1'

- PIP INT_XOY119 EL2BEG0 -> BYP4

3.693.214

3.693.216

3.693.810

3.693.813

4 configuration memory bits.

In order to have the PIP these bits must be fixed at logic value '1'

Real Coding Xilinx Virtex-5LX50T

31

- PIP INT_XOY119 SE2END2 -> FAN7

3.693.213

3.693.214

3.693.831

3.693.835

4 configuration memory bits.

In order to have the PIP these bits must be fixed at logic value '1'

- PIP INT_XOY119 EL2BEG0 -> BYP4

3.693.214

3.693.216

3.693.810

3.693.813

4 configuration memory bits.

In order to have the PIP these bits must be fixed at logic value '1'

Real Coding Xilinx Virtex-5LX50T

32

Xilinx FPGA Editor - \\vboxsrv\shared_win7\Xilinx_Validation_Projects\test.ncd - [Array1]

File Edit View Tools Window Help

PIP INT_X0Y119 SE2END2 -> FAN7

An upset in the bit 3.693.214 (1->0) may open two different PIPs

PIP INT_X0Y119 EL2BEG0 -> BYP4

The image shows a screenshot of the Xilinx FPGA Editor interface. The main window displays a complex routing diagram with numerous white lines representing connections on a black background. A vertical pink line is visible on the left side. A blue text box is overlaid on the diagram, containing the text: "An upset in the bit 3.693.214 (1->0) may open two different PIPs". Two ovals are drawn on the diagram: a red one on the left and a green one on the right, both pointing towards the blue text box. The window title bar shows "Xilinx FPGA Editor - \\vboxsrv\shared_win7\Xilinx_Validation_Projects\test.ncd - [Array1]" and the menu bar includes "File Edit View Tools Window Help". The toolbar contains various icons for editing and viewing the design.

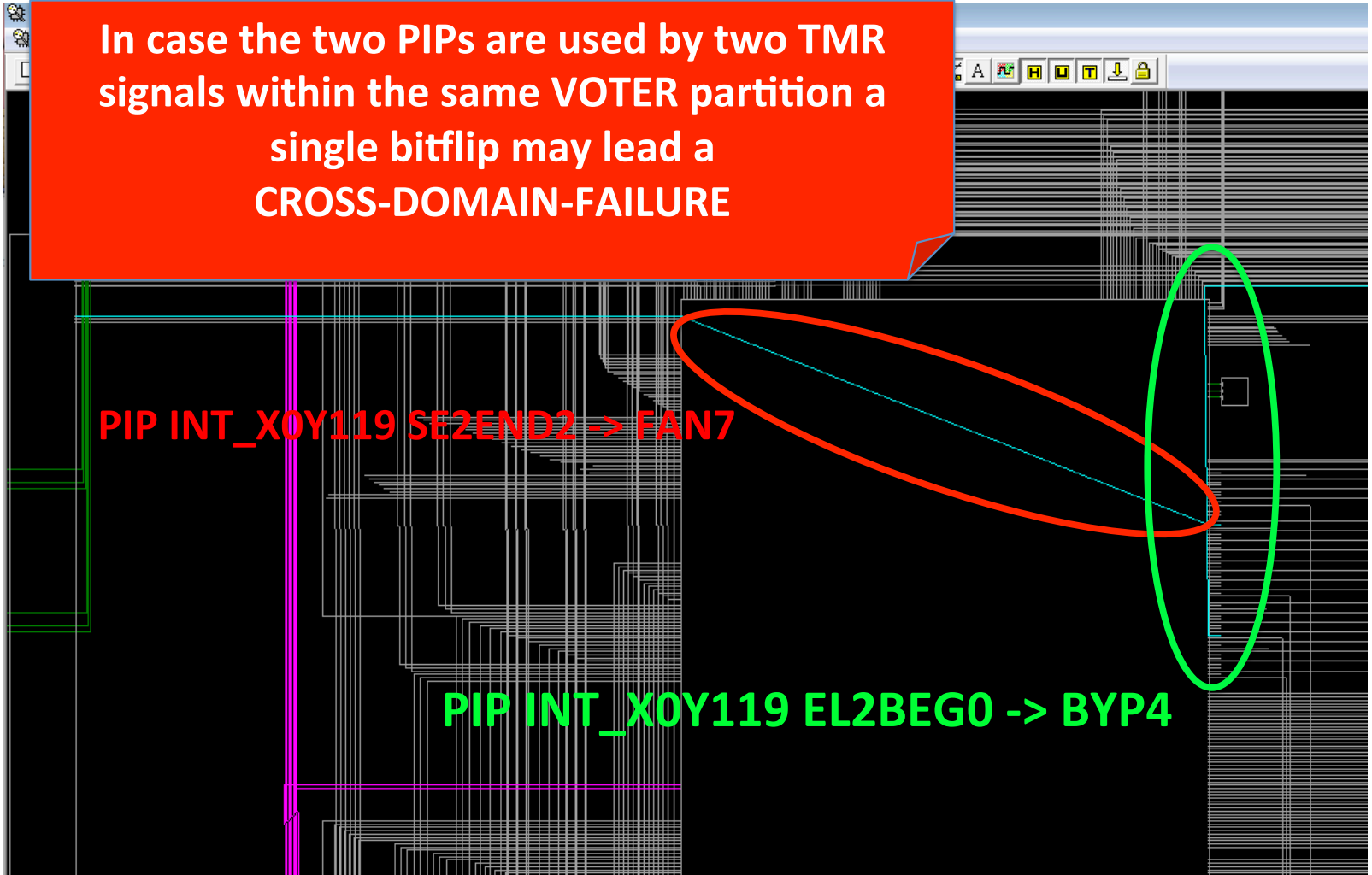
Real Coding Xilinx Virtex-5LX50T

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In case the two PIPs are used by two TMR signals within the same VOTER partition a single bitflip may lead a CROSS-DOMAIN-FAILURE

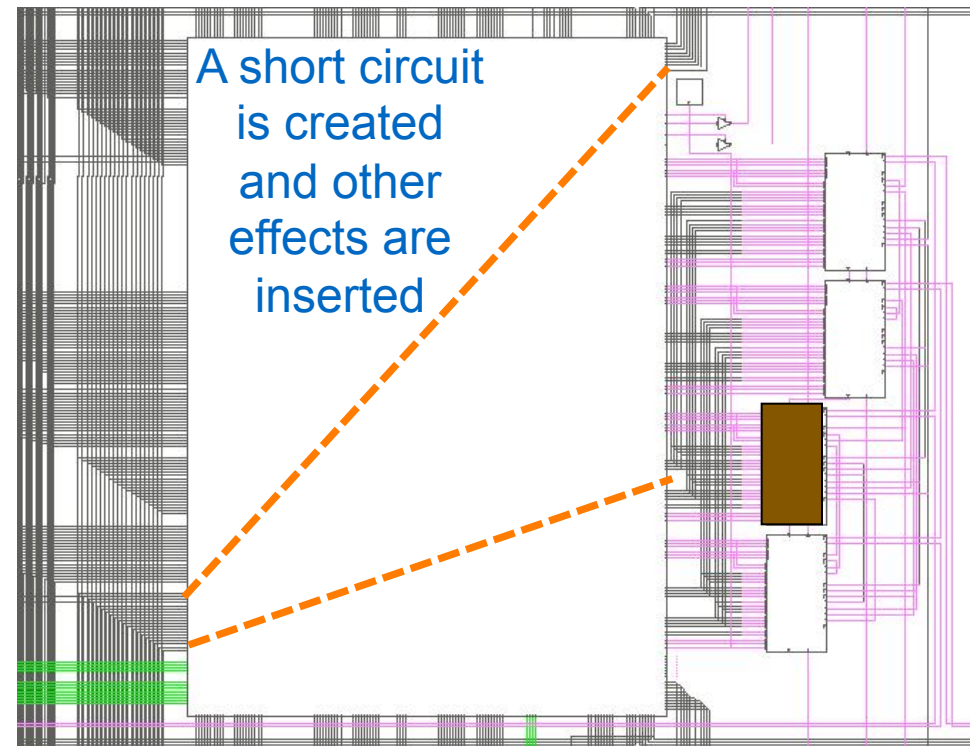
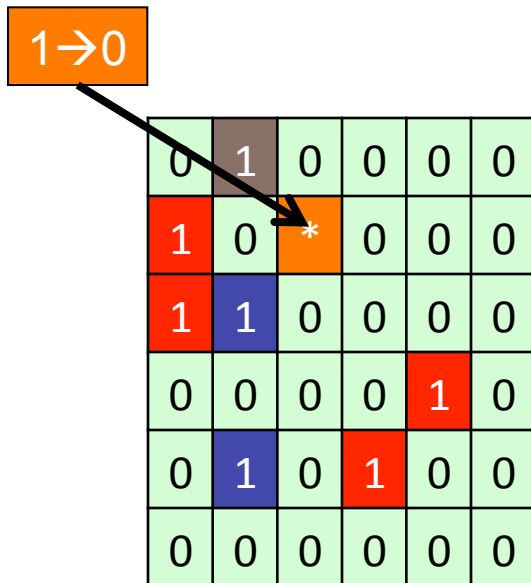
PIP INT_X0Y119 SE2END2 -> FAN7

PIP INT_X0Y119 EL2BEG0 -> BYP4



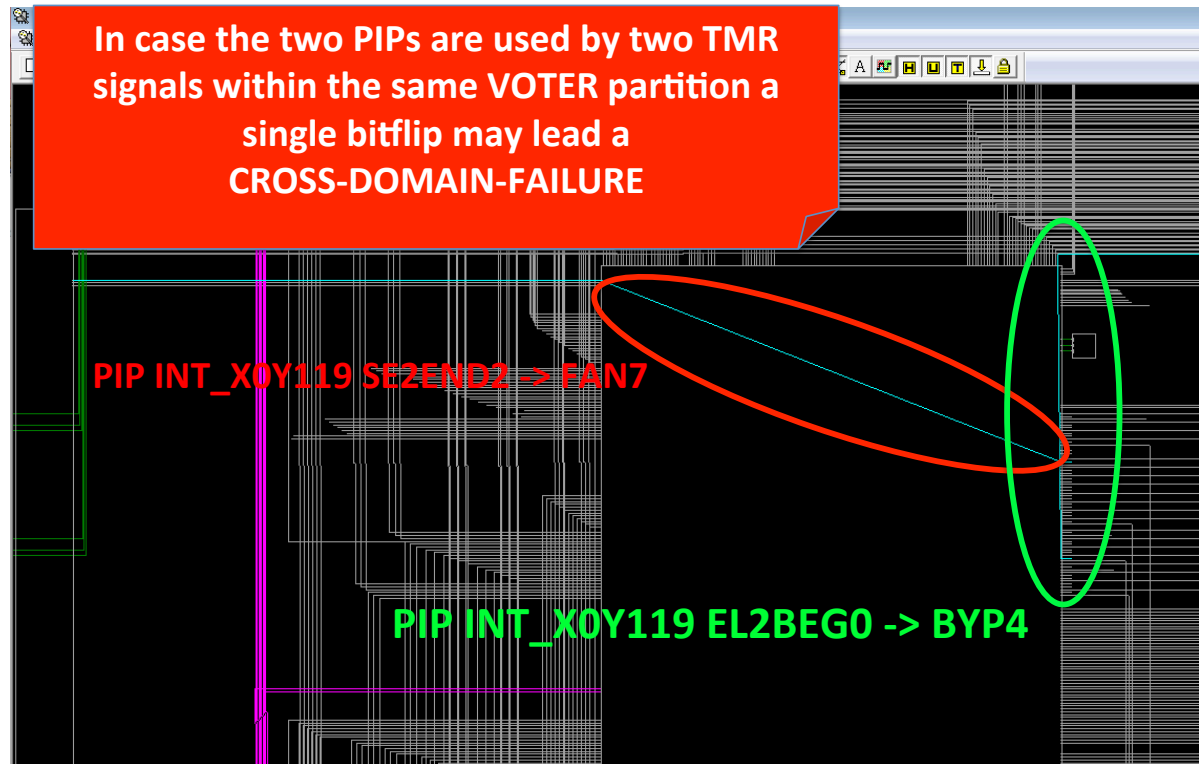
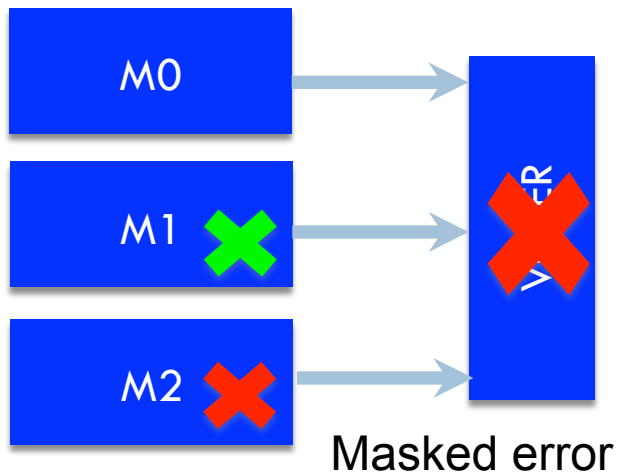
1-bit controlling multiple PIPs

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Real Coding Xilinx Virtex-5LX50T

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Results and Classification

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- Identification of all the architecturally relevant sensitive bits
 - If affected, these configuration memory bits may change the physical structure of the circuit

Results and Classification

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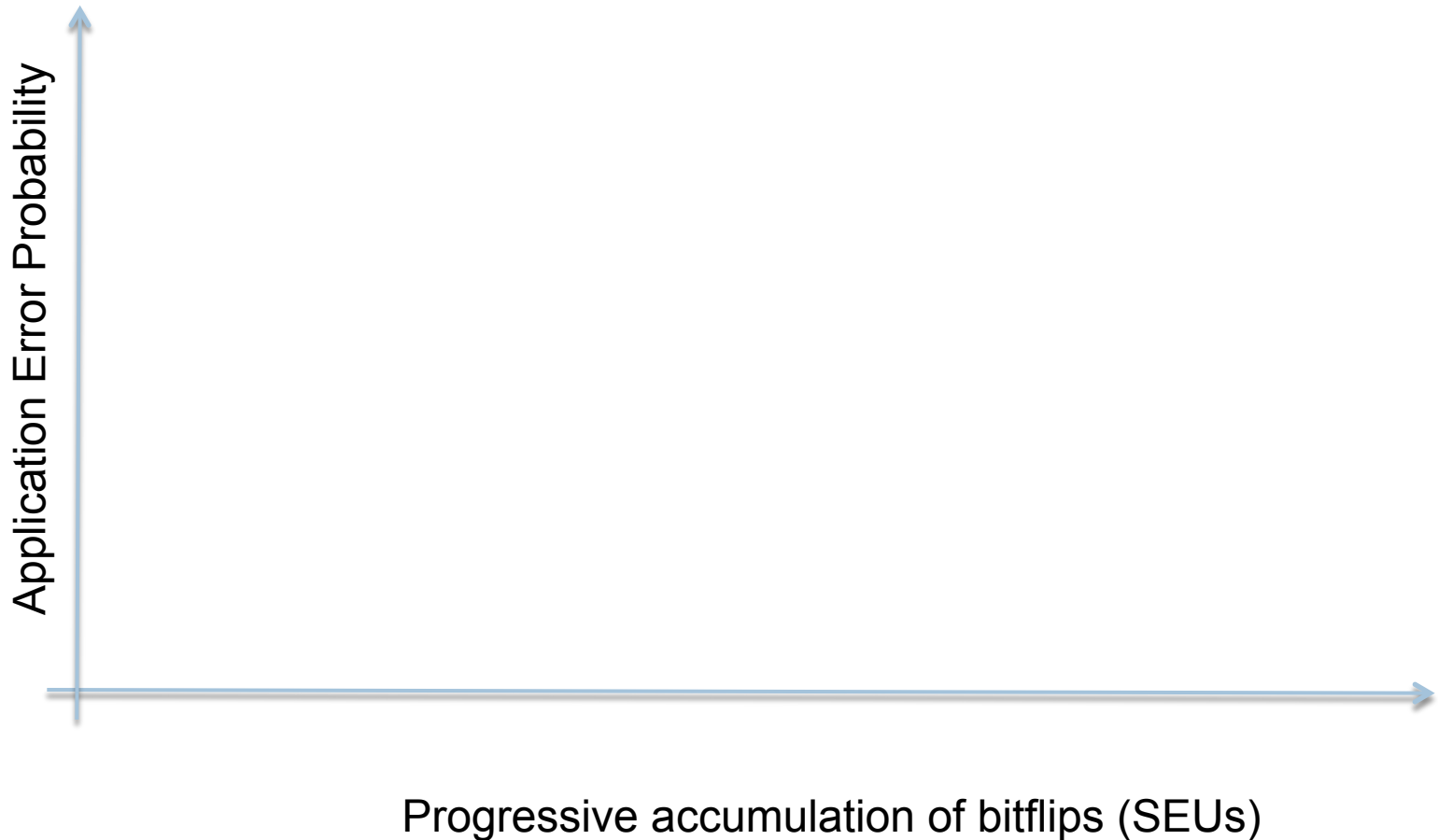
- Identification of the configuration memory bits that if affected generate a **Single Point of Failure (SPF)**

```
-- Bit Reference 13661788 Location X 60 Y 186
-- TMR Sensitive ID 1 X 60 Y 186
-- Domain 0 - Net 1: net "uAHBUART/count_reg_TR0<20>"
--           - PIP 1:   pip INT_X60Y186 BYP_BOUNCE5 -> IMUX_B29
-- Domain 1 - Net 2: net "uAHBUART/count_reg_TR1<20>"
--           - PIP 2:   pip INT_X60Y186 WL2BEG1 -> IMUX_B26
```

Results and Classification

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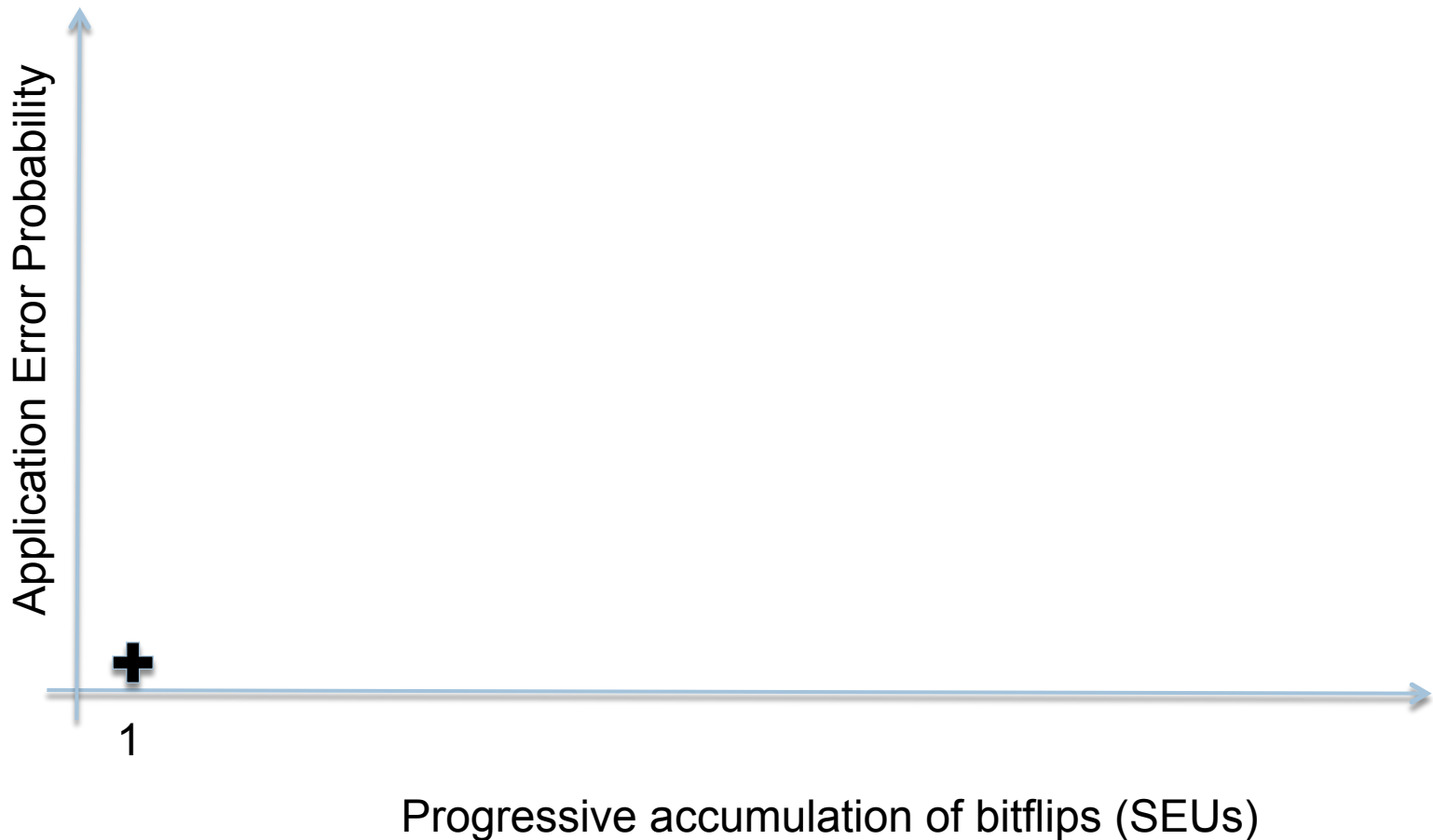
- Calculation of the Application Error Probability



Results and Classification

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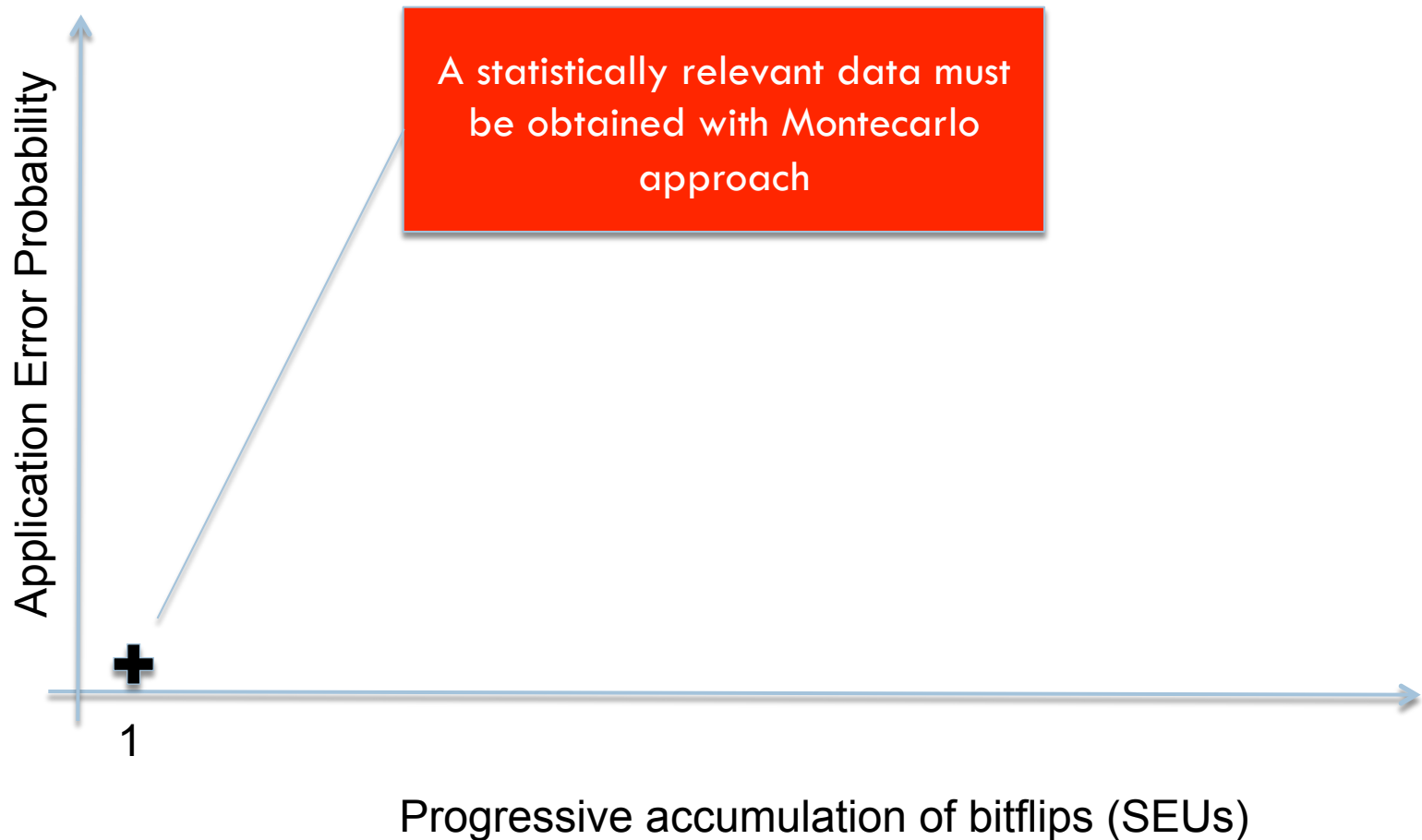
- Calculation of the Application Error Probability



Results and Classification

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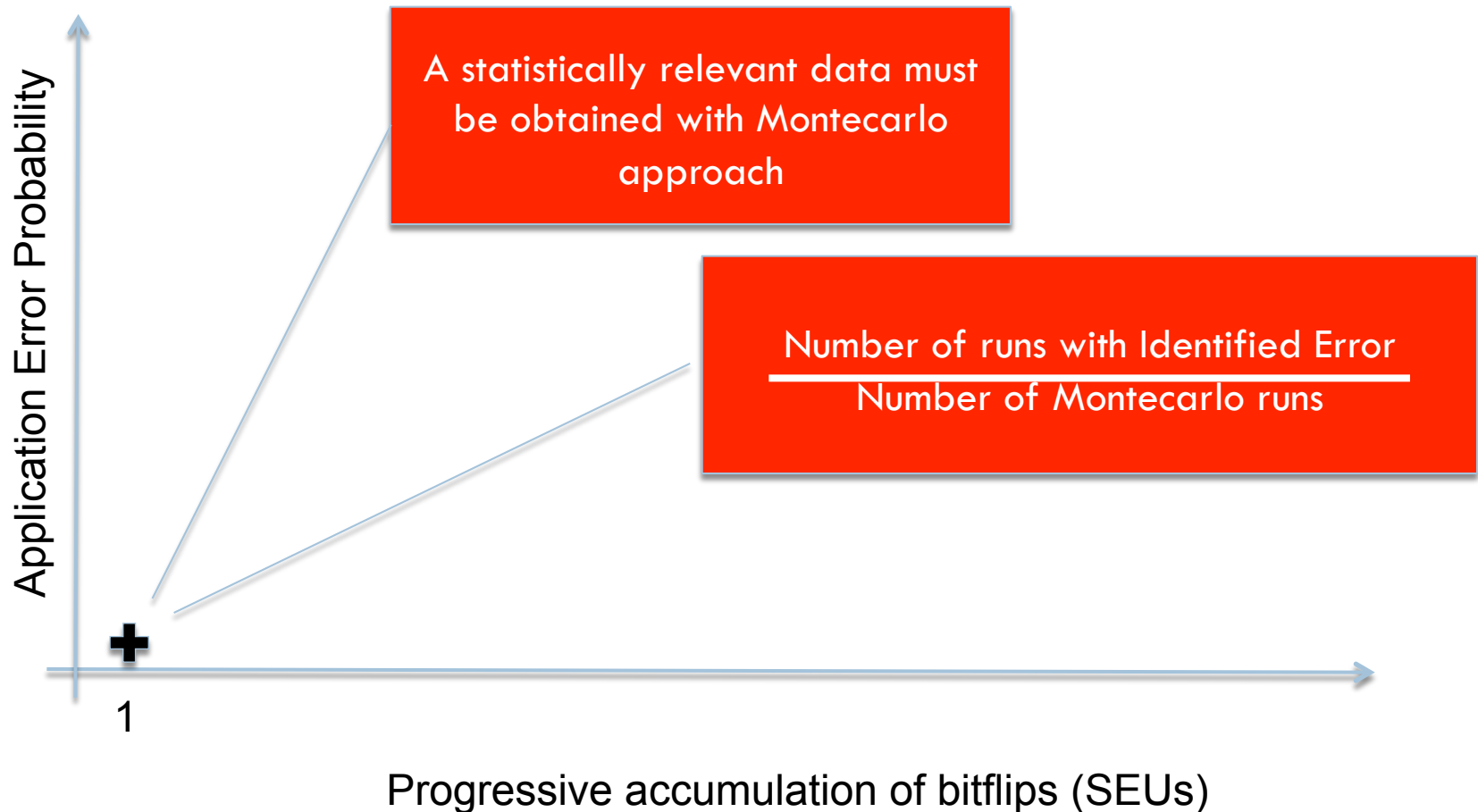
□ Calculation of the Application Error Probability



Results and Classification

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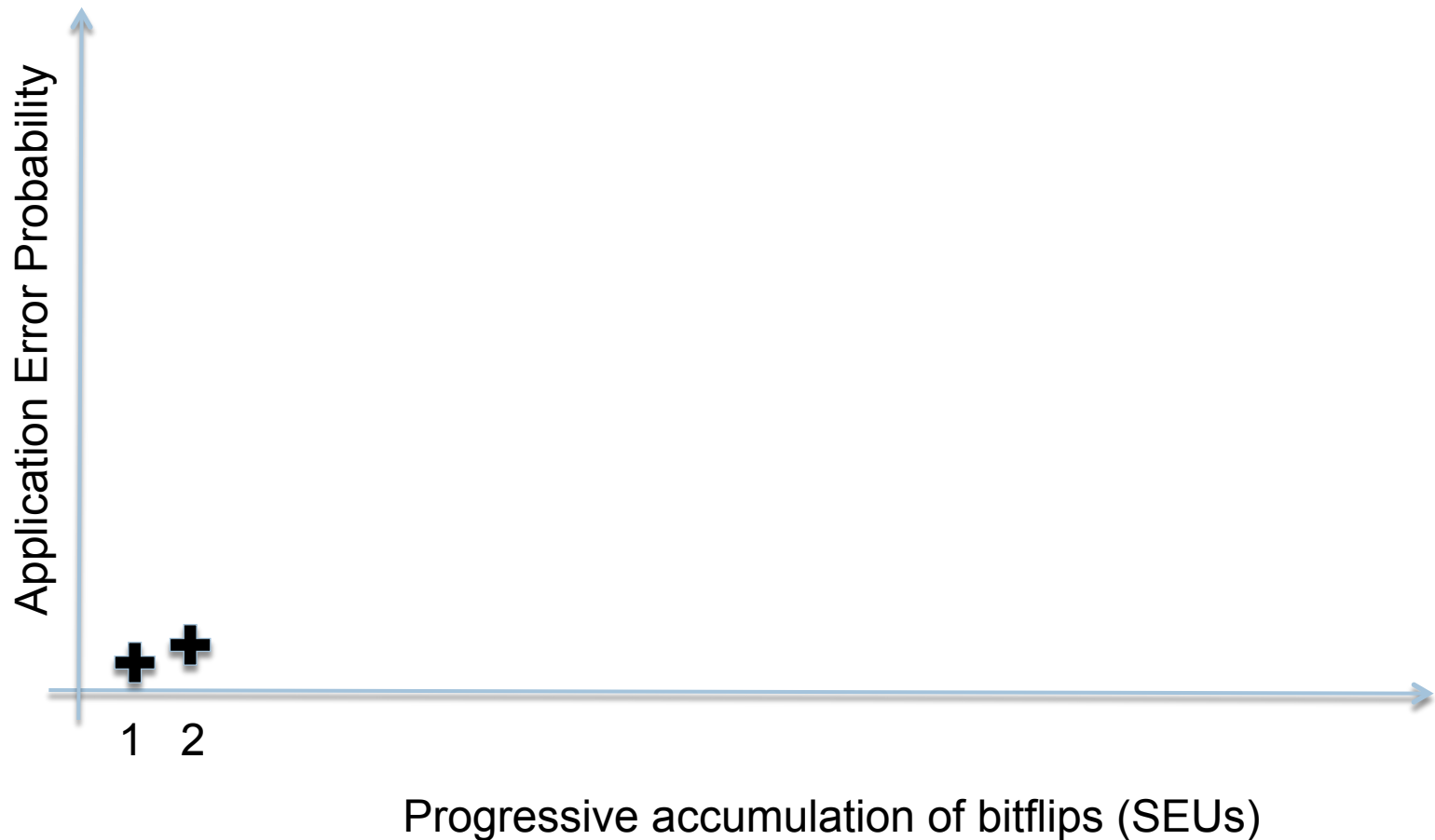
□ Calculation of the Application Error Probability



Results and Classification

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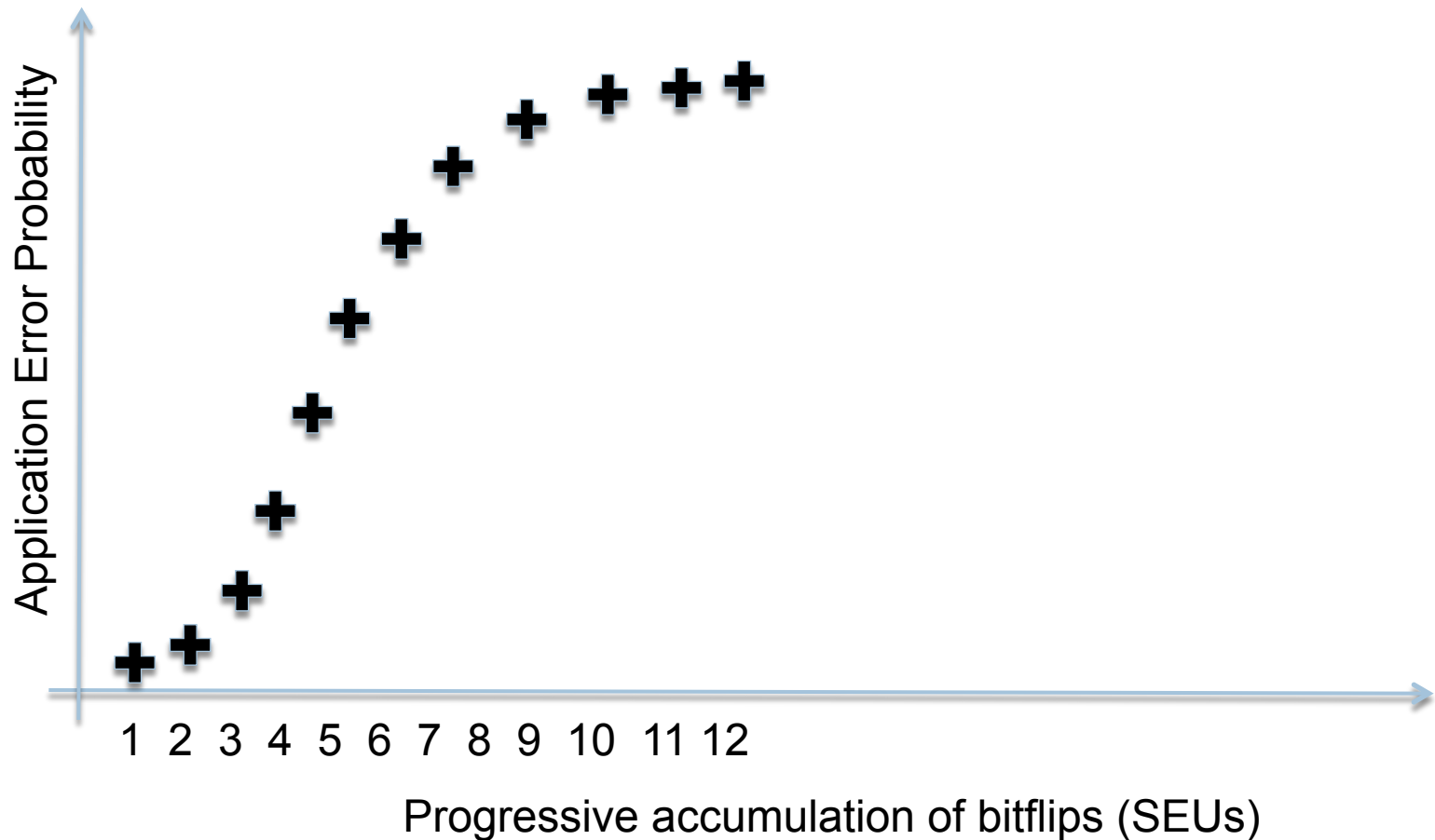
- Calculation of the Application Error Probability



Results and Classification

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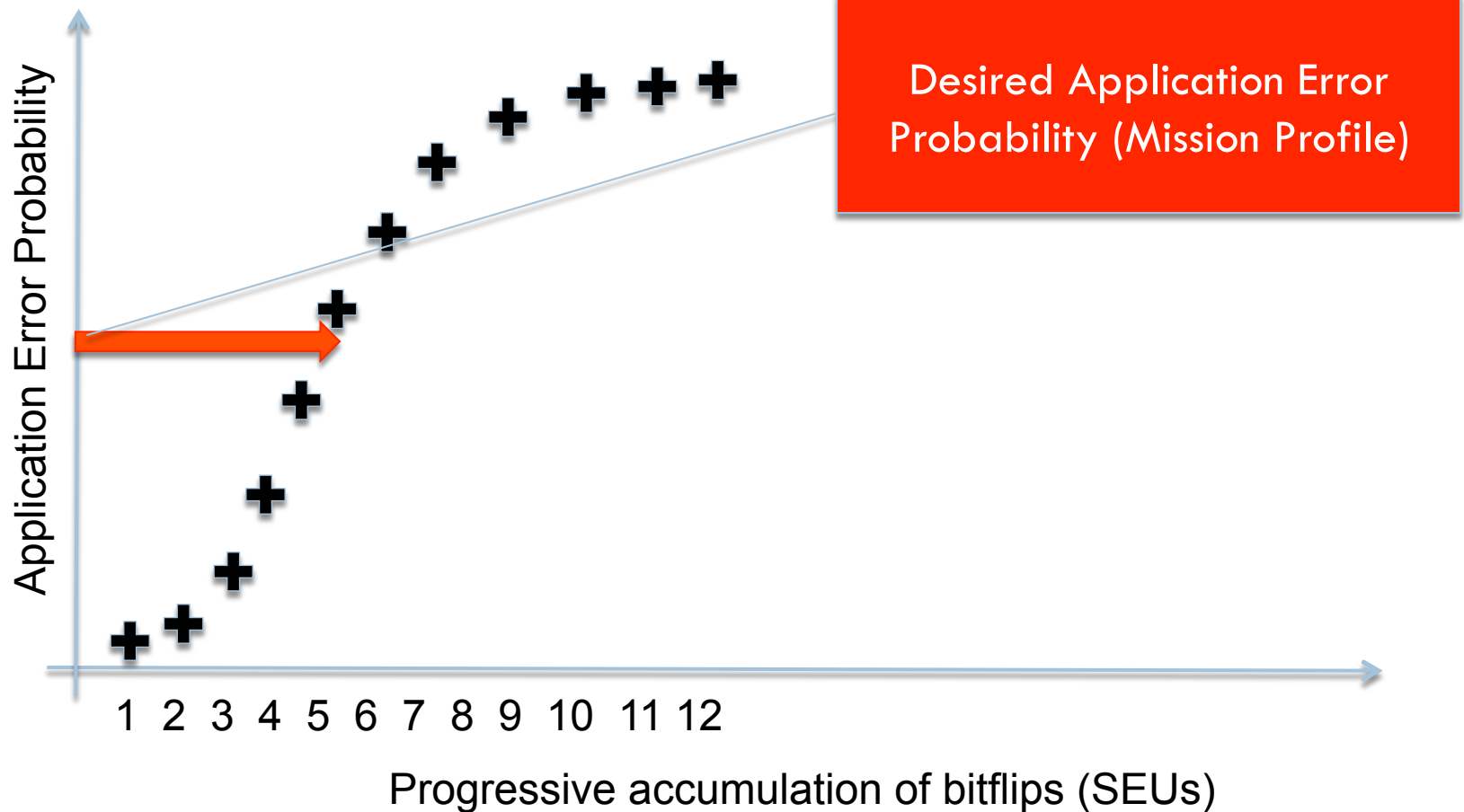
- Calculation of the Application Error Probability



Results and Classification

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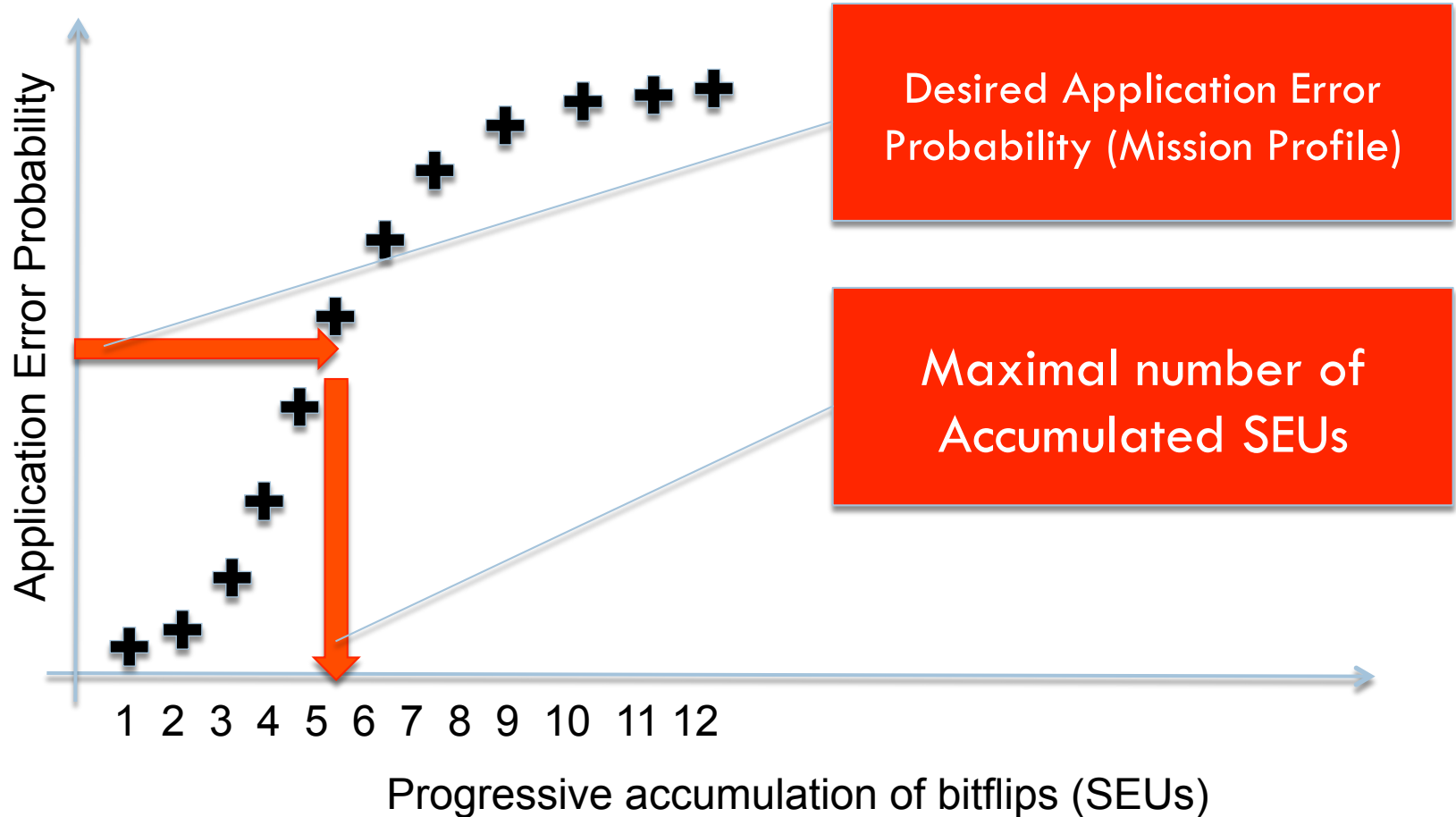
□ Calculation of the Application Error Probability



Results and Classification

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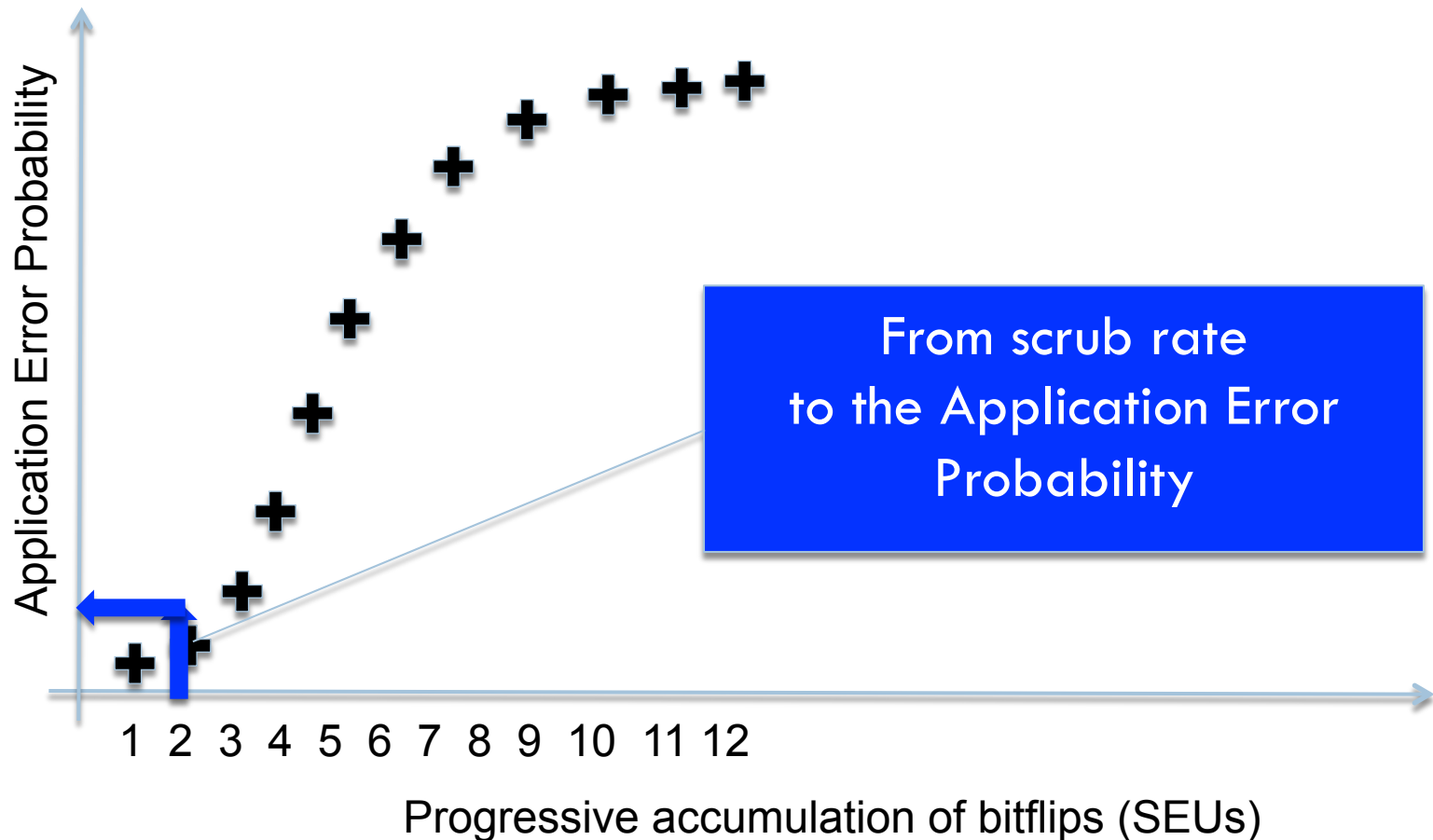
□ Calculation of the Application Error Probability



Results and Classification

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- Calculation of the Application Error Probability



Experimental Results

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- B13 from ITC'99 an interface Meteo sensor

B13 circuit characteristics

Name	VHDL		Type	Gate level				Fault list	
	# Line	# Process		Gates	Pi	Po	FF	Complete	Collapse
B13	296	5	std	362	10	10	53	1,906	830
			opt	317	10	10	53	1,694	77

B13 Test Patterns details

Circuit	# Sequences	# Vectors	Fault Coverage %	Fault detected	Fault Total
B13	5	7639	81.27	1341	1650

Experimental Results

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- Area occupation on Xilinx Virtex-5 LX50T FPGA

Circuit	Design Topology	PLAIN	XTMR	VP-XTMR
B13	Slice FF	62/28800 - 1%	147/28800 - 1%	147/28800 - 1%
	Slice LUTs	84/28800 - 1%	369/28800 - 1%	369/28800 - 1%
	Slices Distribution	42/7200 - 1%	177/7200 - 2%	177/7200 - 2%
B13 x 30	Slice FF	1590/28800 - 5%	4770/28800 - 16%	4770/28800 - 16%
	Slice LUTs	1830/28800 - 6%	10,841/28800 - 37%	10,841/28800 - 37%
	Slice Distribution	827/7200 - 11%	4791/7200 - 66%	4791/7200 - 66%

Experimental Results

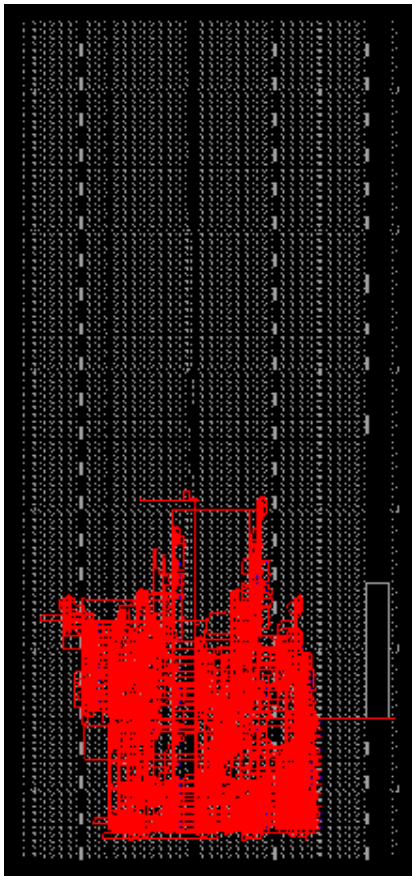
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- 3 different design topologies have been tested at Los Alamos
 - **PLAIN** : b13x30 without any type of hardening
 - **XTMR**: Triple Modular Redundancy version with converge option of outputs pins using Xilinx TMRTool 2.1.76
 - **VP-XTMR**: Hardening version of XTMR with replacement constraints generated byVERI-Place tool.

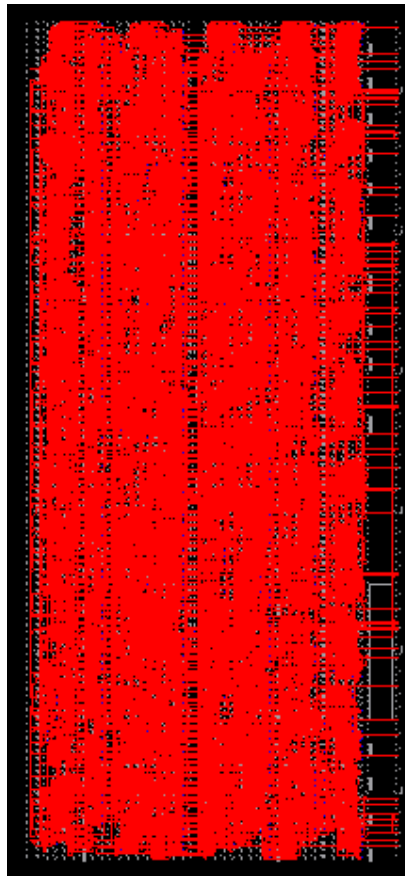
Experimental Results

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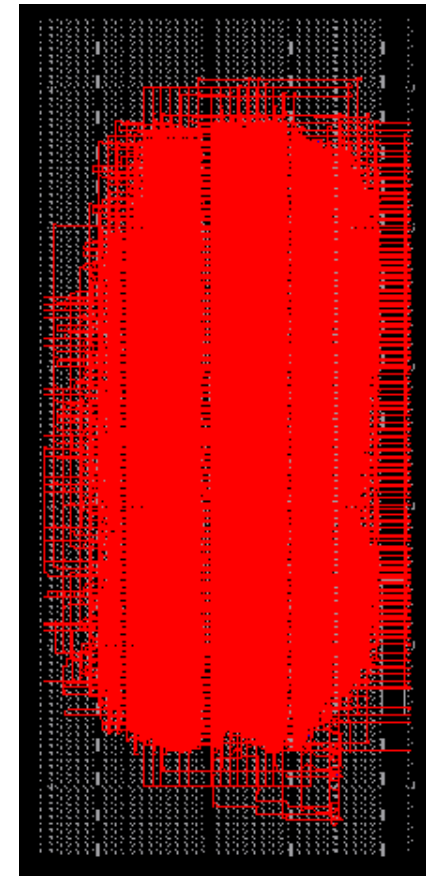
B13x30 - PLAIN



B13x30 - XTMR



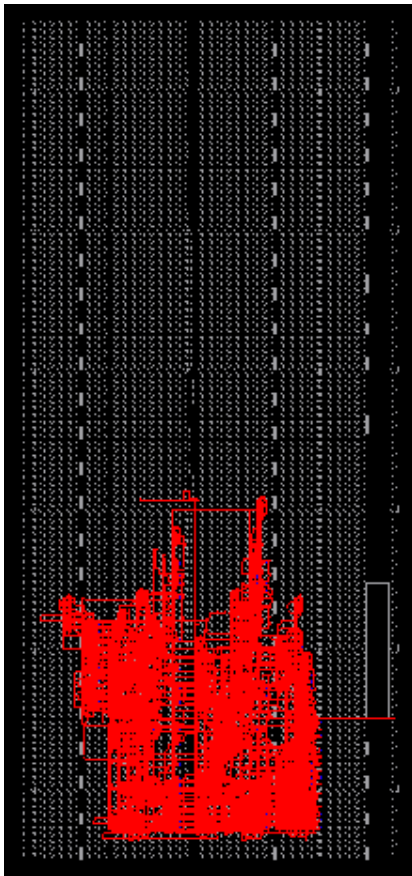
B13x30 - VP-XTMR



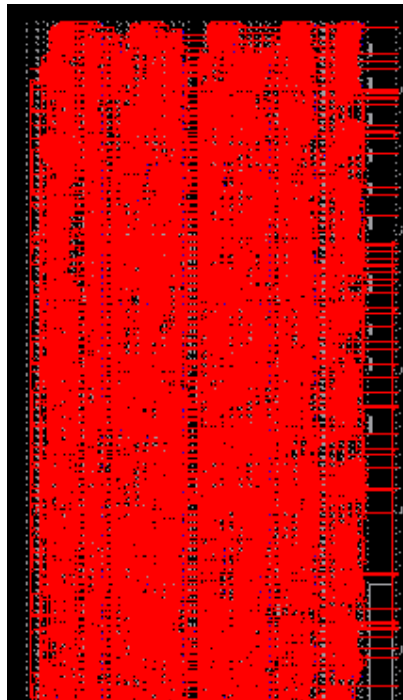
Experimental Results

51

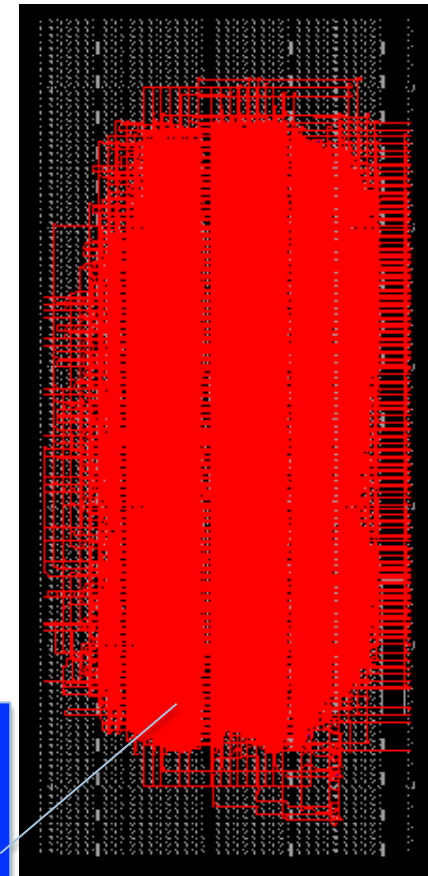
B13x30 - PLAIN



B13x30 - XTMR



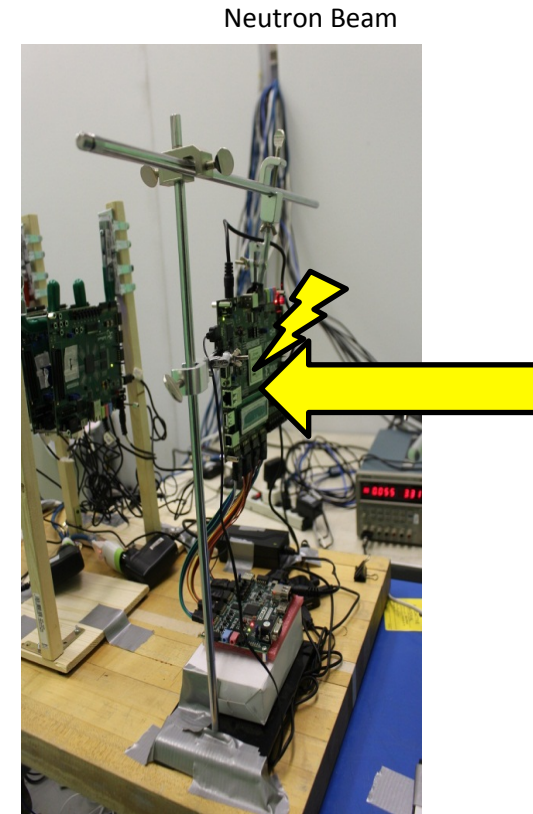
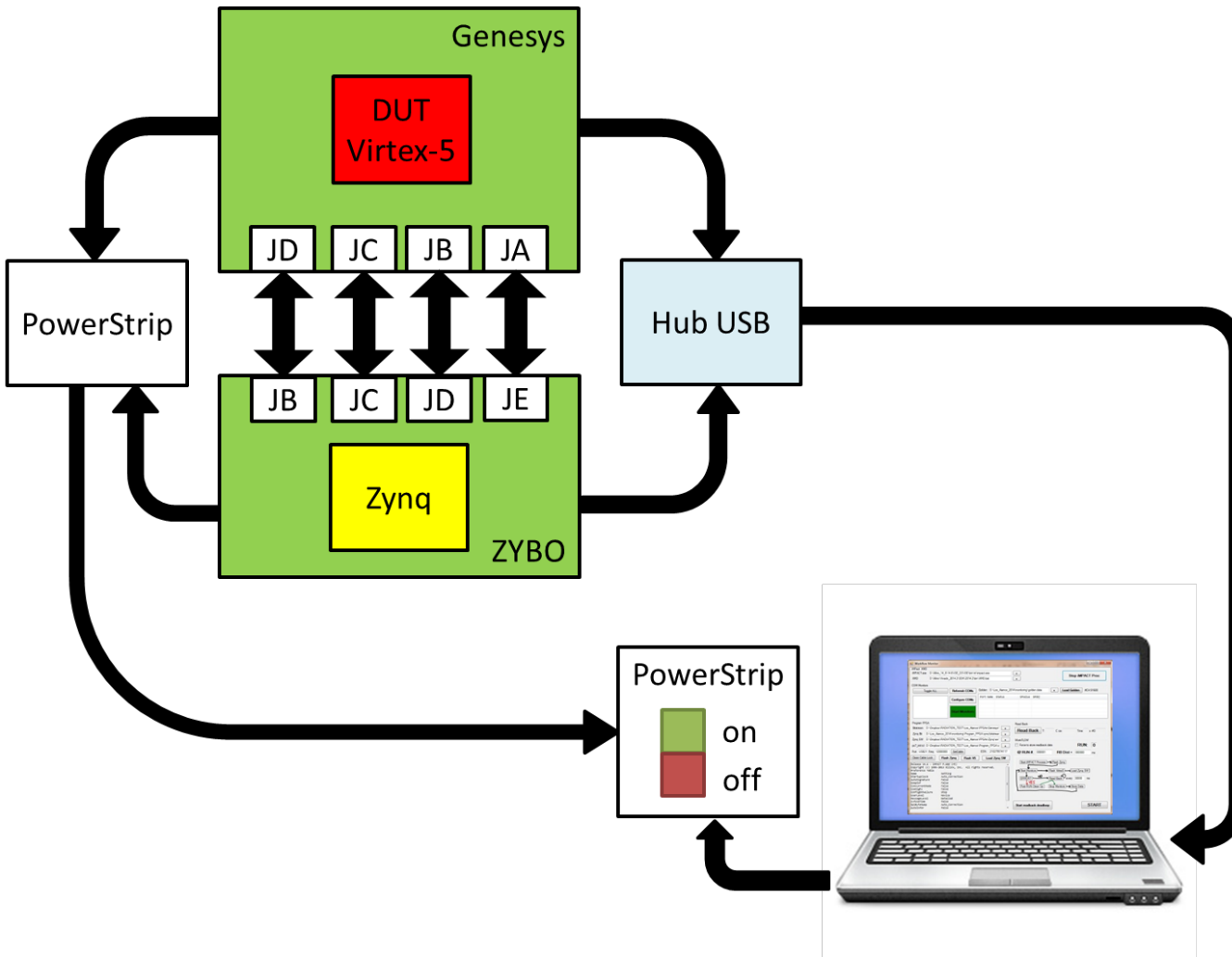
B13x30 - VP-XTMR



The Layout is complementary
with Isolation Design Flow

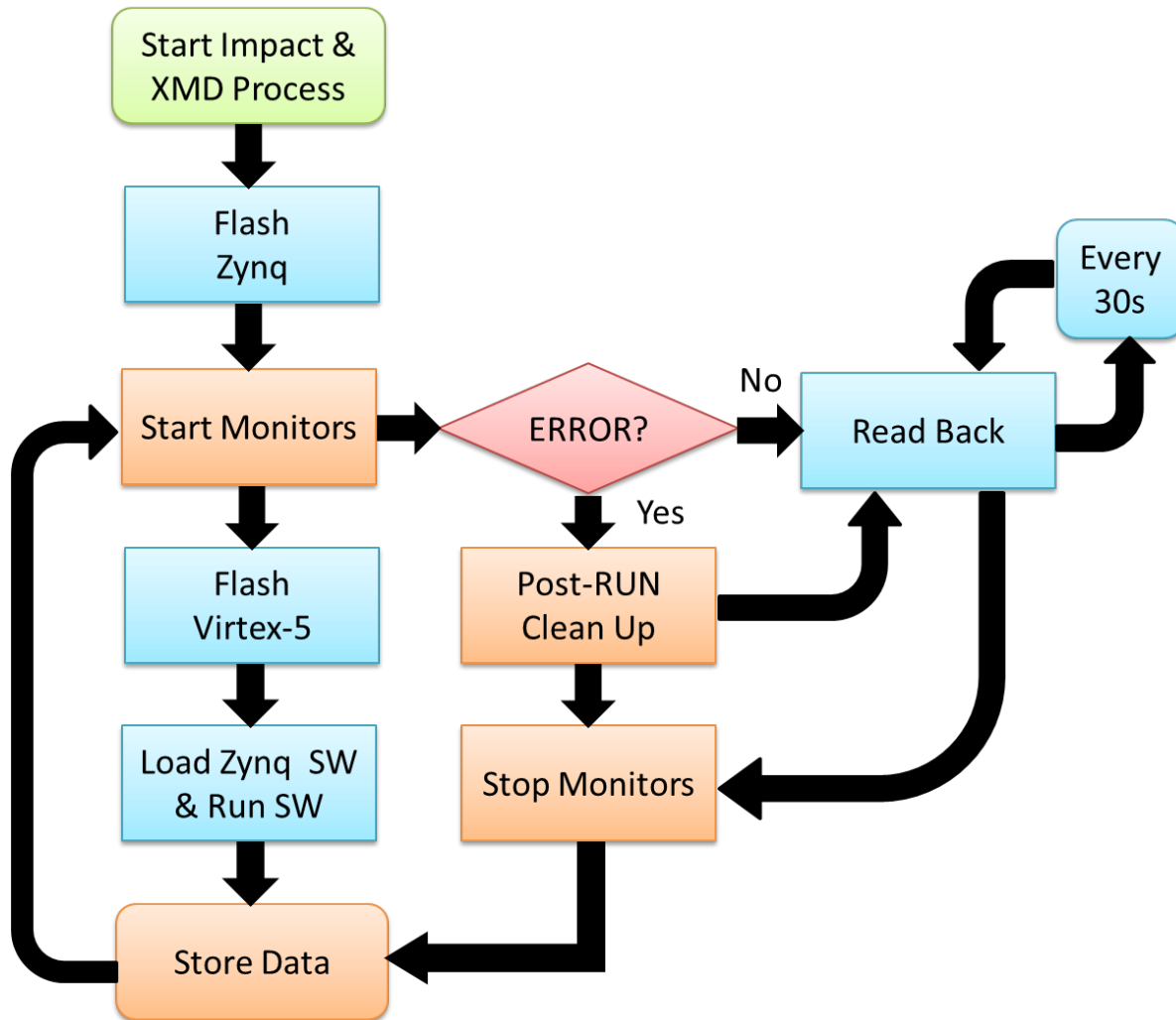
Experimental Results

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Test Methodology

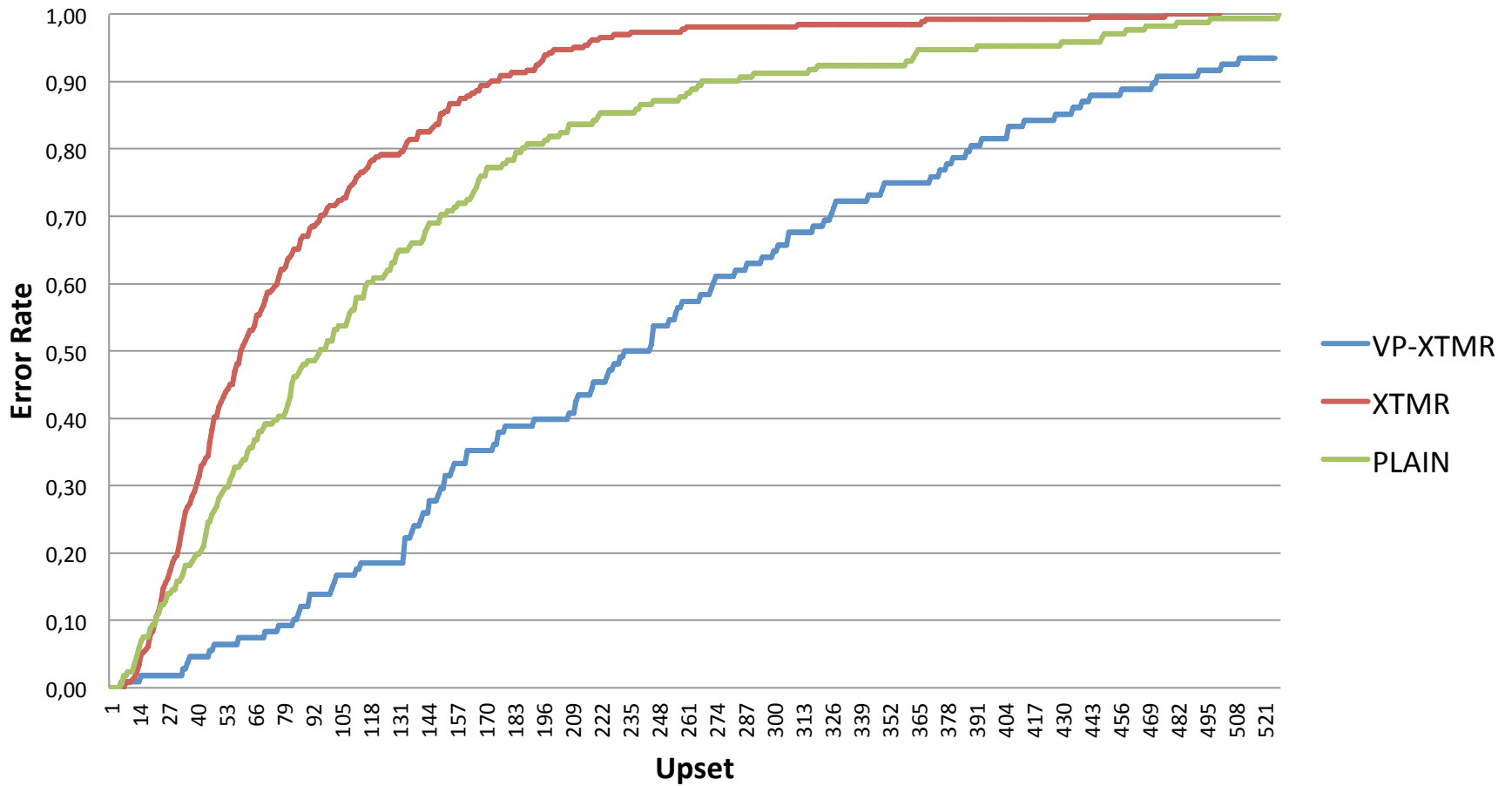
53



Experimental results

54

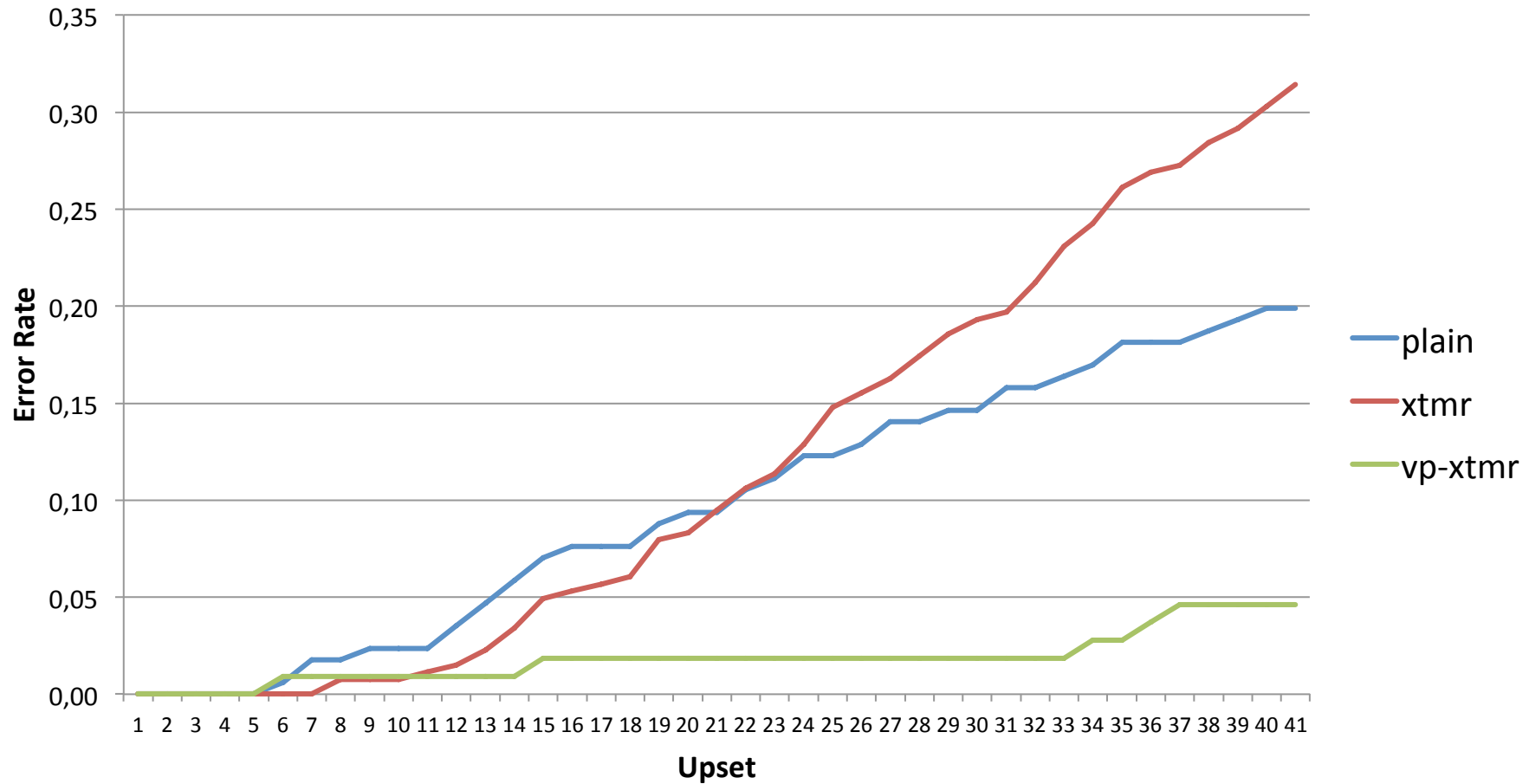
RT: PLAIN - XTMR - VP-XTMR



Experimental results

55

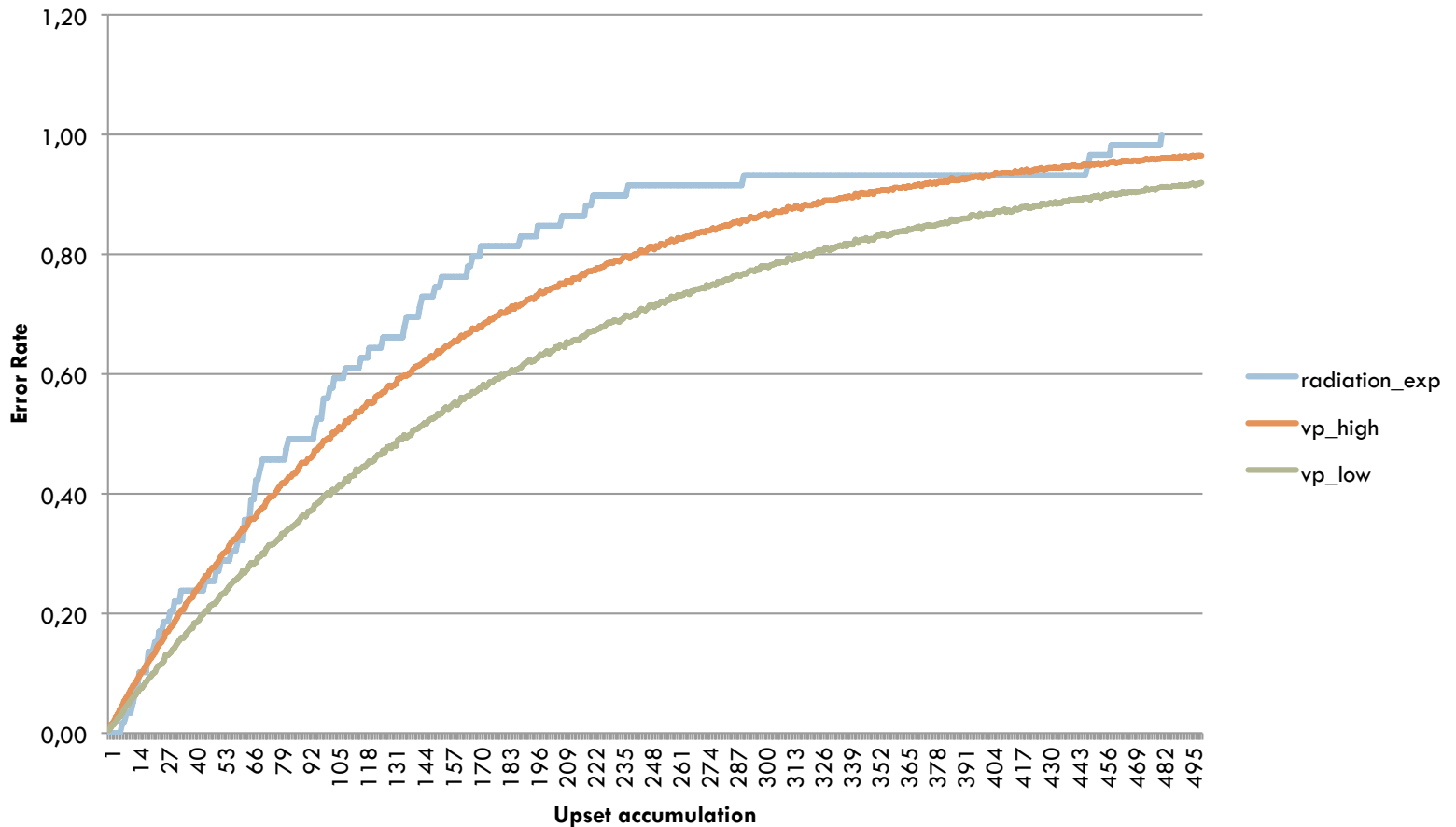
breakeven point



Experimental results – Plain Prediction

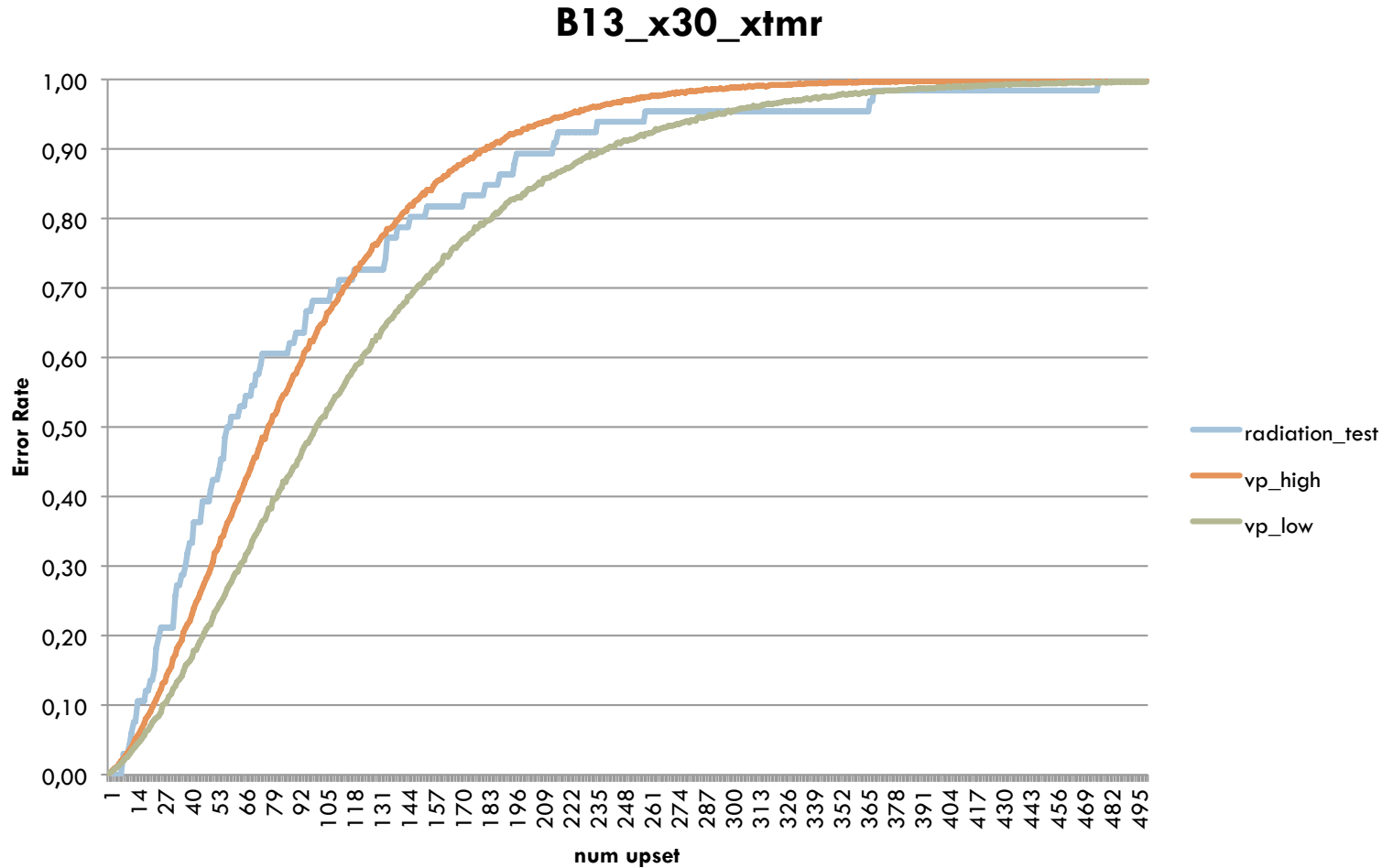
56

b13_x30 plain



Experimental results – XTMR Prediction

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Experimental results – ARM-M0

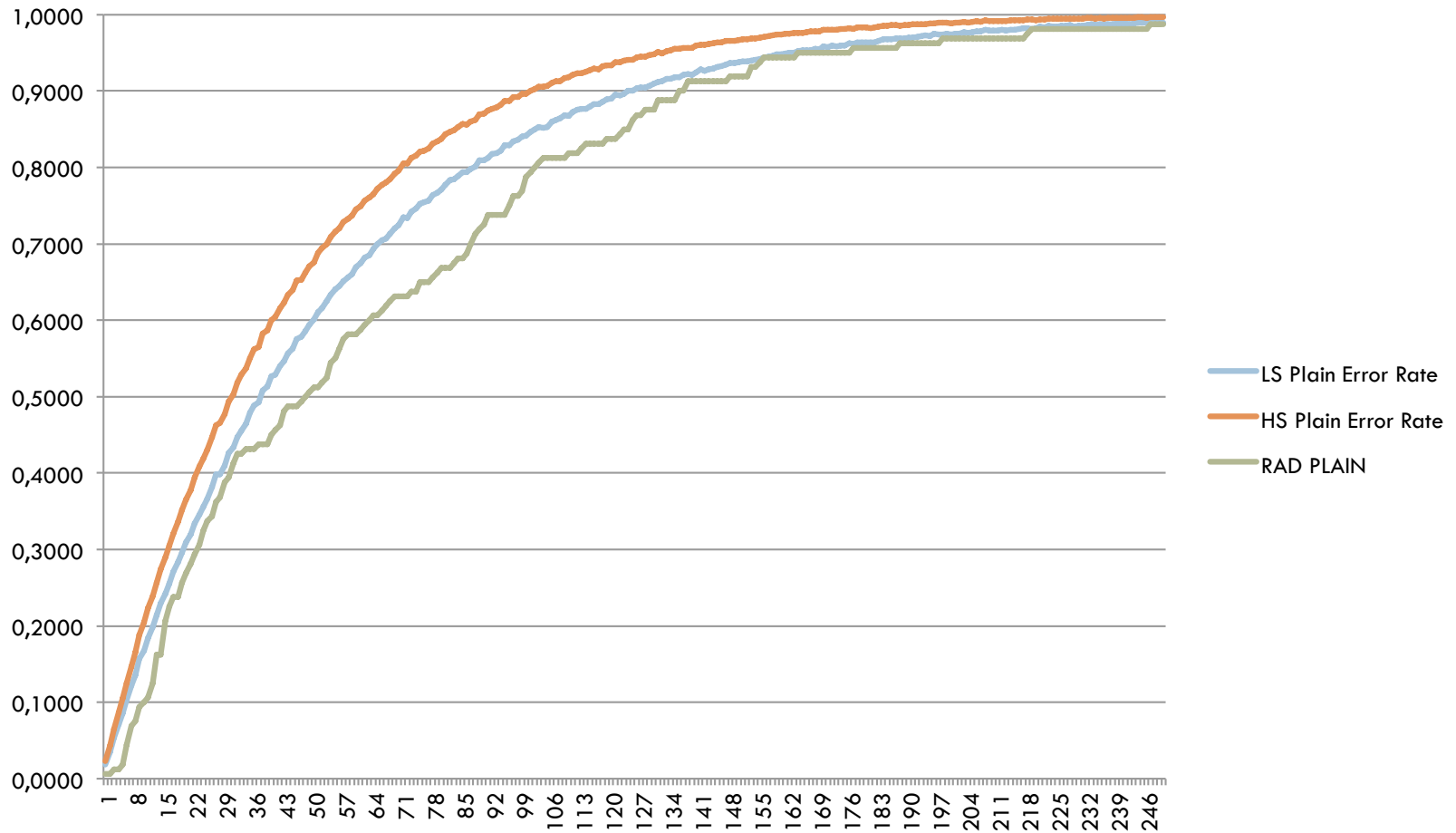
58

- ARM-M0 processor has been tested at PSI
 - Available flux of proton: $7.22E6$ [p/(cm²s)]
 - Working frequency of 50 Mhz
 - Software: Bubble sort

Design Version	LUTs[#]	FFs[#]	BRAM[#]
<i>Plain</i>	3563 (12%)	961 (3%)	4 (6%)
<i>XTMR</i>	13,229 (45%)	2887 (10%)	12 (20%)
<i>XTMR-VP</i>	13,229 (45%)	2887 (10%)	12 (20%)

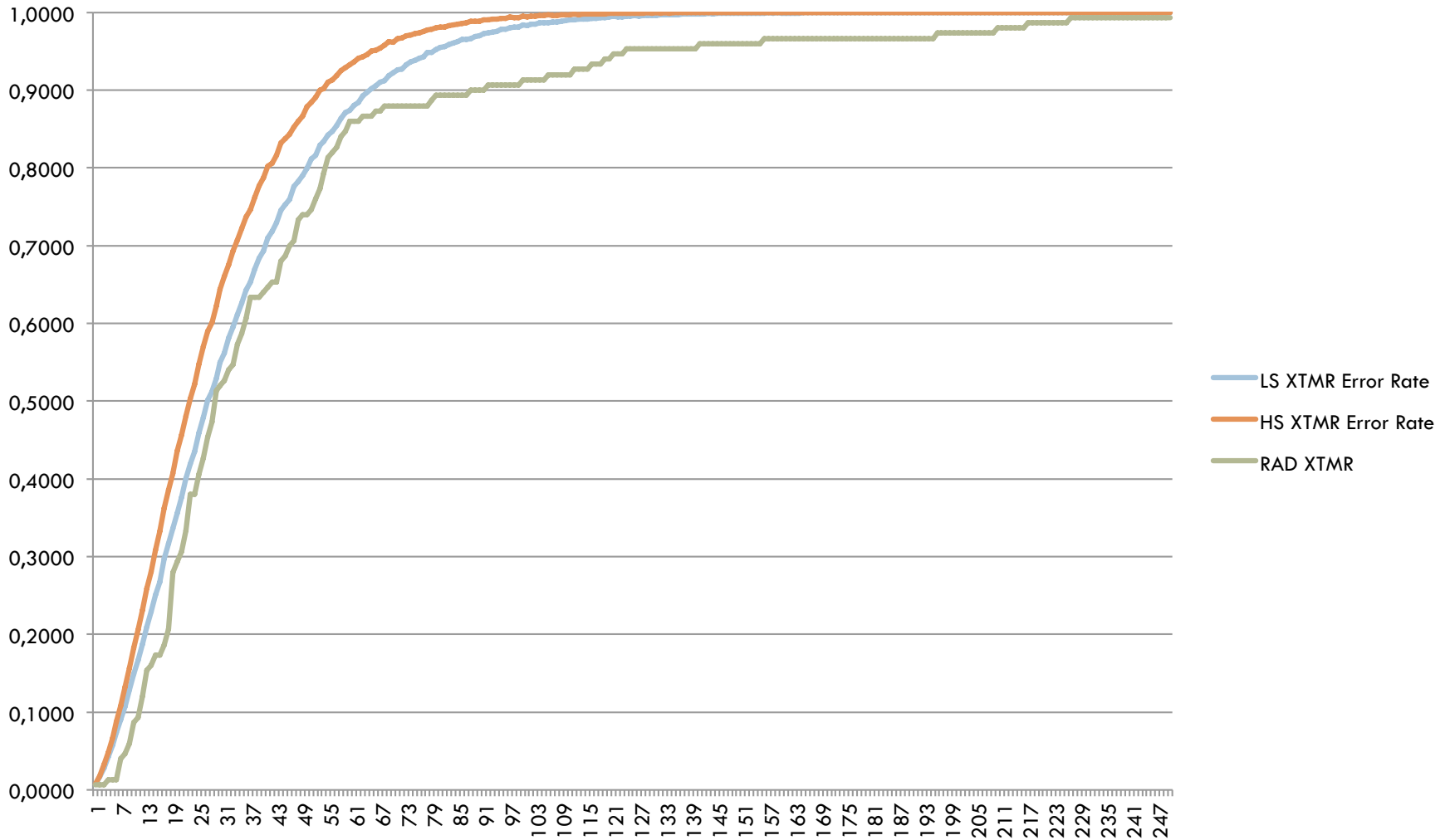
Experimental results – ARM Plain prediction

59

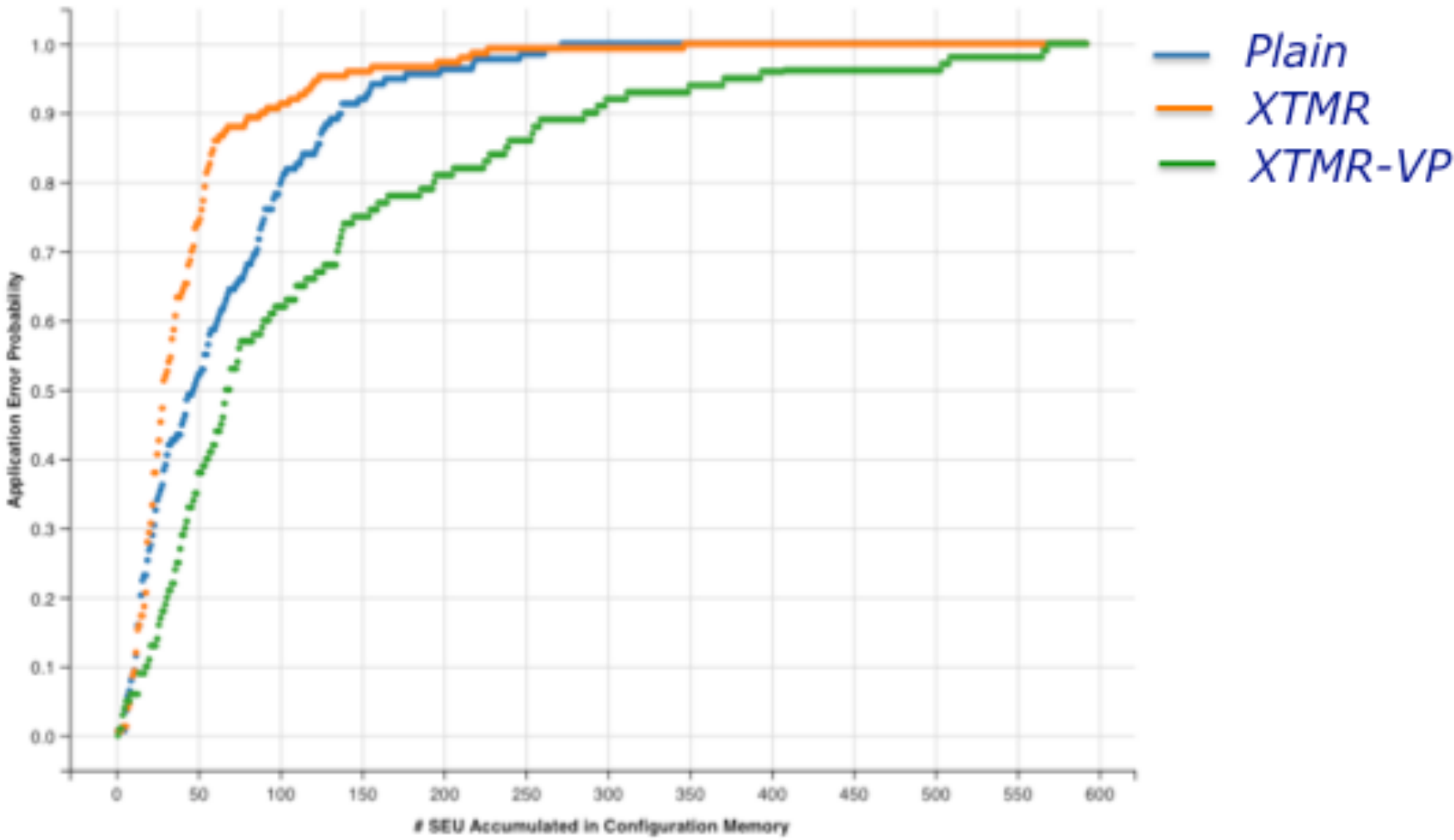


Experimental results – ARM XTMR Prediction

60



Experimental results – ARM overall results



Conclusions and future works

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- VERI-Place for Virtex-5LX50T is available online
 - Fault injection tests executed
 - Radiation test validate VERI-Place
 - Specific versions released to some users
- VERI-Place is available for Zynq family
- VERI-Place for Kintex7-X7K325T is available upon request
 - Fault injection is ongoing
 - Radiation test is planned

Thank you!

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