Accurate Analysis of SET effects on Flash-based FPGA System-on-a-Chip for Astrophysical Applications

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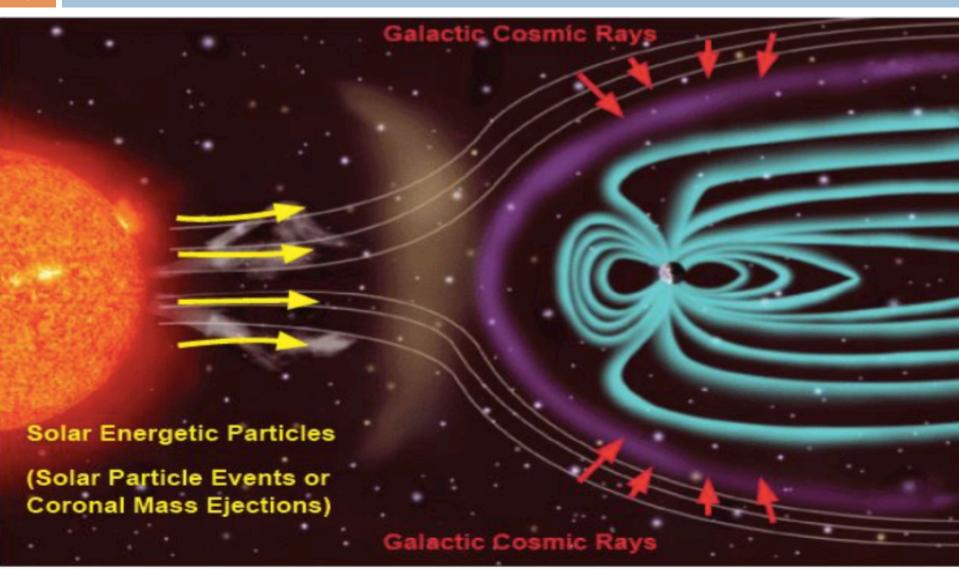




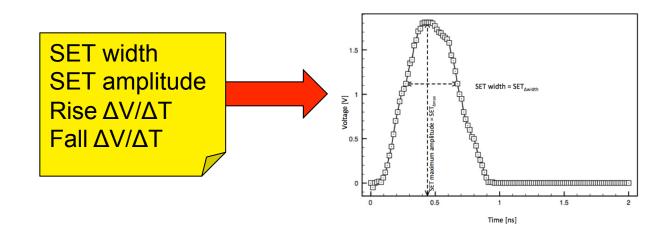


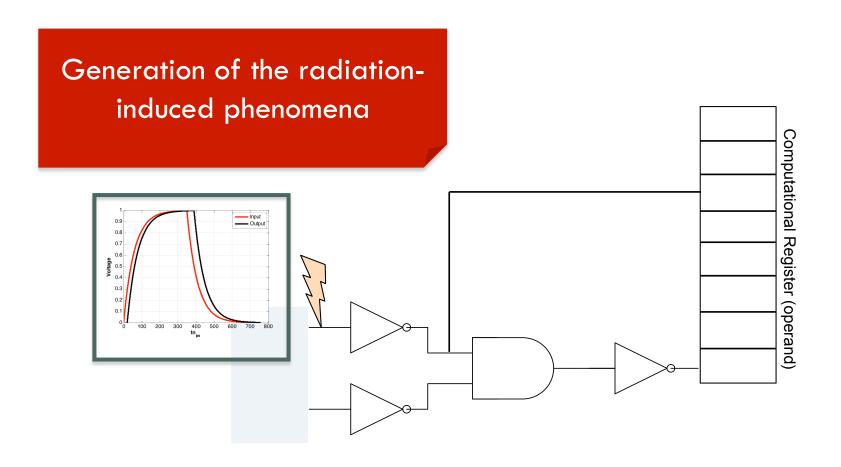
Outline

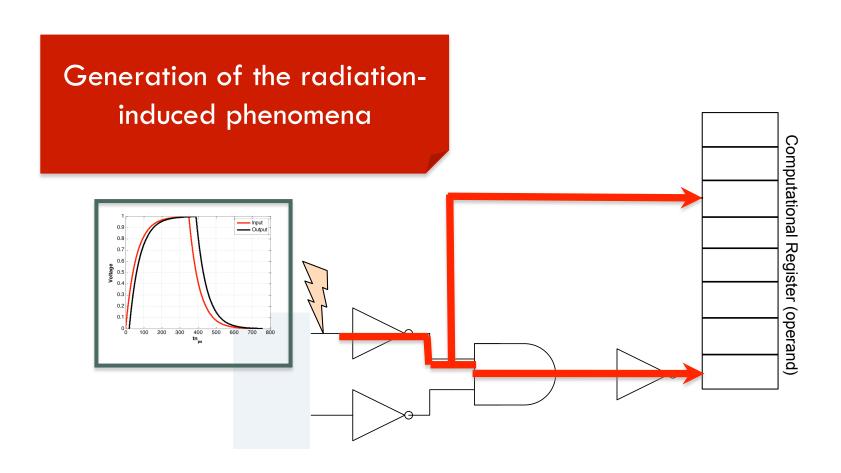
- SET effects on Flash-based FPGAs
- Single Event Transient Analysis (SETA) tool
 - Analysis
 - Mitigation
 - Experimental results
- Conclusions and future activities



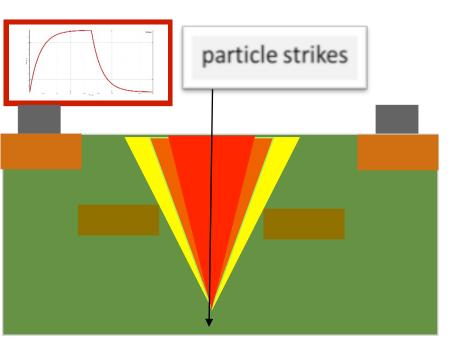
- A Single Event Transient (SET) is generated by the injunction of charge collection
 - A charged particle crosses a junction area
 - It generates an amount of current, provoking a "glitch"
 - SET can be indistinguishable from normal signal and exist for notable distances

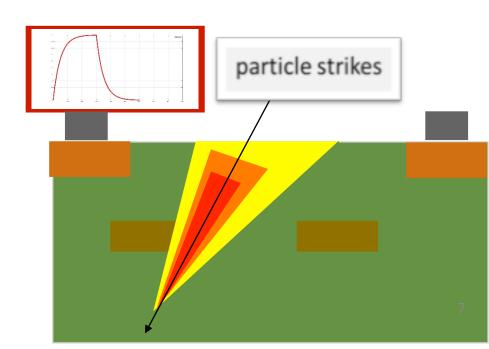






- Analysis and mitigation of the SEEs on Flash-based FPGAs
 - Type and radiation incidence angle
 - LET
 - Technology

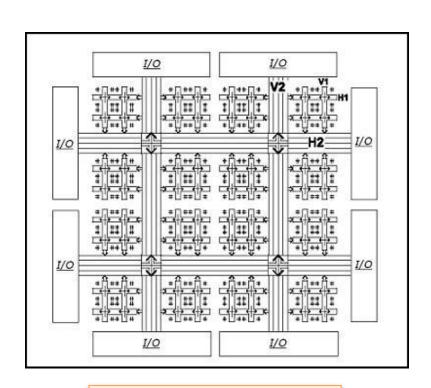




Circuits on Flash-based FPGAs

0	0	0	0	0	0
0	0	0	0	0	0
0	0	0	0	0	0
0	0	0	0	0	0
0	0	0	0	0	0
0	0	0	0	0	0

Flash configuration memory

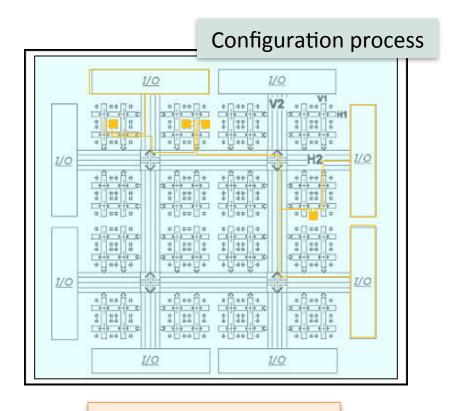


FPGA array

Circuits on Flash-based FPGAs

0	1	0	0	0	0
1	0	0	0	0	0
1	1	0	0	0	0
0	0	0	0	1	0
0	1	0	1	0	0
0	0	0	0	0	0

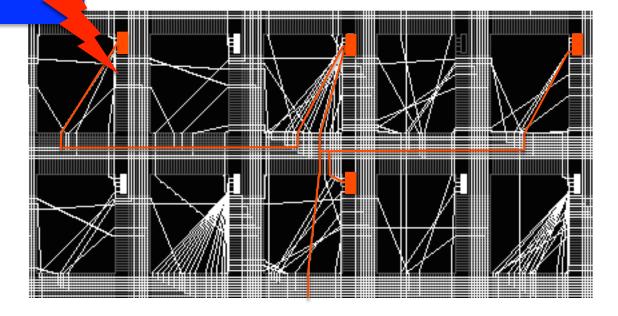
Flash configuration memory



FPGA array

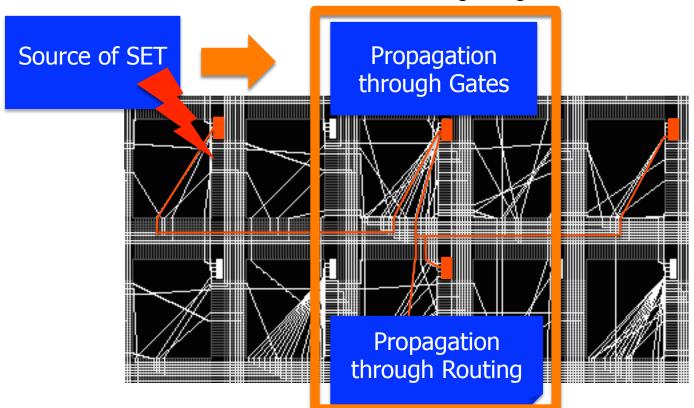
SET scenario

- Considering a place and route design on FPGA
 - □ Fixed logic cells
 - Defined number of routing segments



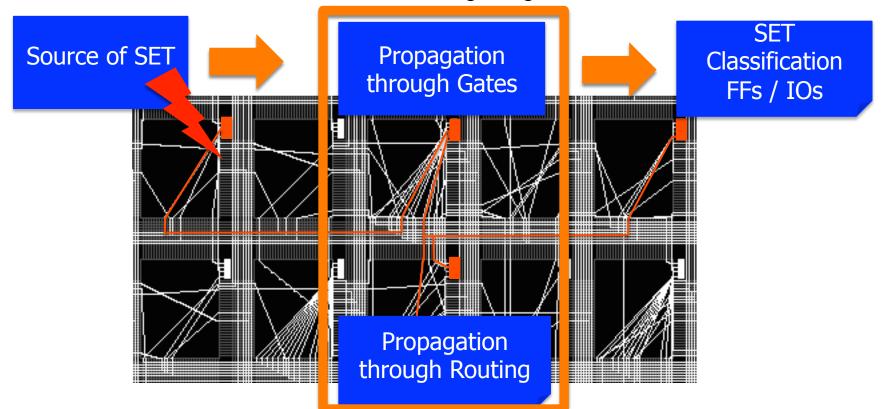
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SET scenario

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SET Propagation through gates

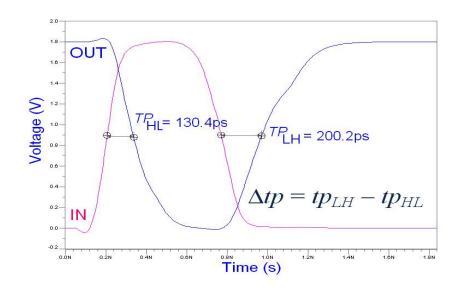
Fist Region: If $(\tau_n < k^*tp)$ then $\tau_{n+1} = 0$

[Wirth et al, NSREC 2008]

Second Region: If $(\tau_n > (k+3)^*tp)$ then $\tau_{n+1} = \tau_n + \Delta tp$

Third Region: If $((k+1)*tp < \tau_n < (k+3)*tp)$ then $\tau_{n+1} = (\tau_n^2 - tp^2)/\tau_n + \Delta tp$

Fourth Region: If $(k*tp < \tau_n < (k+1)*tp)$ then $\tau_{n+1} = (k+1)*tp(1 - e^{(k-(\tau n/tp))}) + \Delta tp$



For a 1 \rightarrow 0 \rightarrow 1 transition \triangle tp is defined as: \triangle tp = tpHL - tpLH

For a $0 \rightarrow 1 \rightarrow 0$ transition Δtp is defined as: $\Delta tp = tpLH - tpHL$

Source of SET
Propagation through gates
Propagation through routing
SET classification on FFs or IOs

SET Propagation through gates

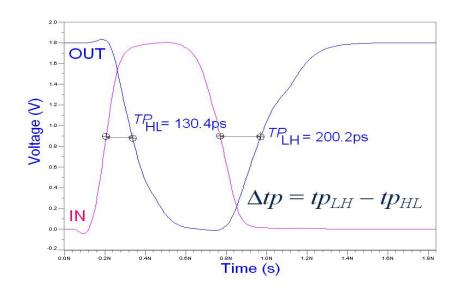
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For a $0 \rightarrow 1 \rightarrow 0$ transition Δtp is defined as: $\Delta tp = tpLH - tpHL$

Source of SET

Propagation through gates
 Propagation through routing
 SET classification on FFs or IOs



G2 - G4

G2 - G3

G3 - G6

G6 – G7

G4 - G5

G5 - FFB

0.070

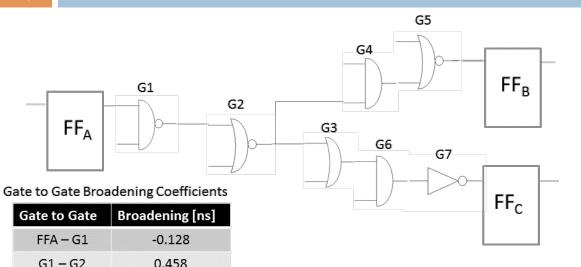
-0.090

0.480

0.140

-0.094

0.130



[Sterpone et al, RADECS 2014]

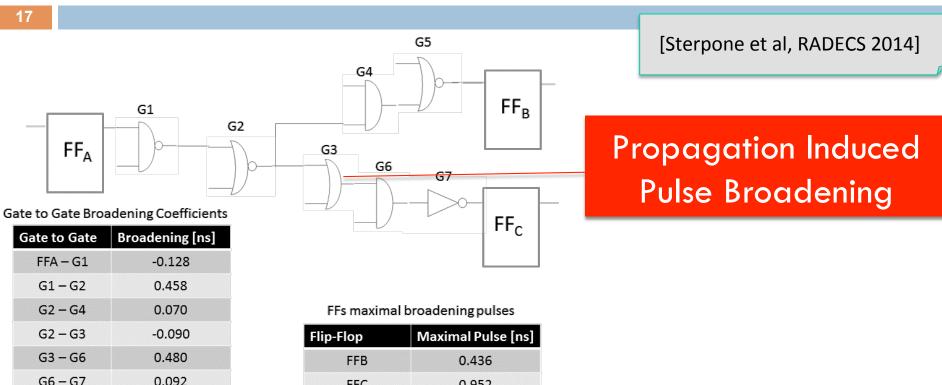
FFs maximal broadening pulses

Flip-Flop	Maximal Pulse [ns]		
FFB	0.436		
FFC	0.952		

Source of SET

Propagation through gatesPropagation through routingSET classification on FFs or IOs

SET Propagation through routing



0.952

FFC

G7 - FFC

G4 - G5

G5 - FFB

0.140

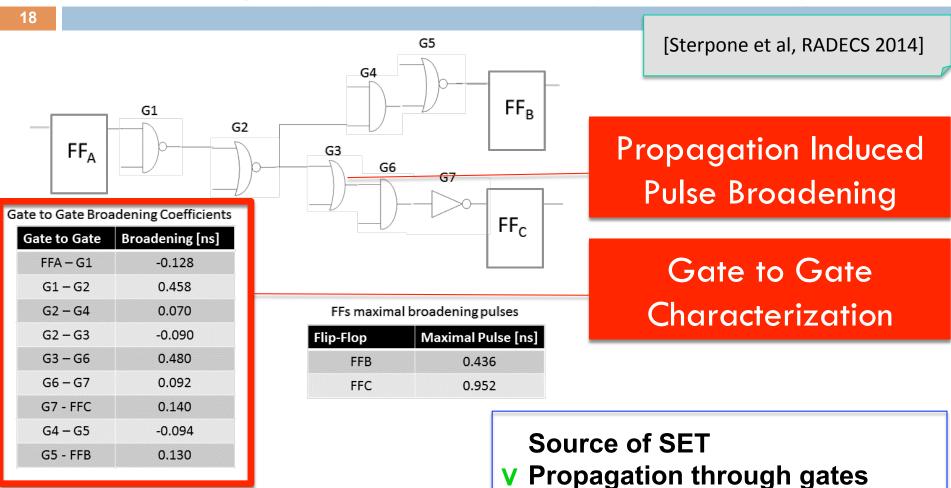
-0.094

0.130

Source of SET

V Propagation through gates **Propagation through routing SET classification on FFs or IOs**

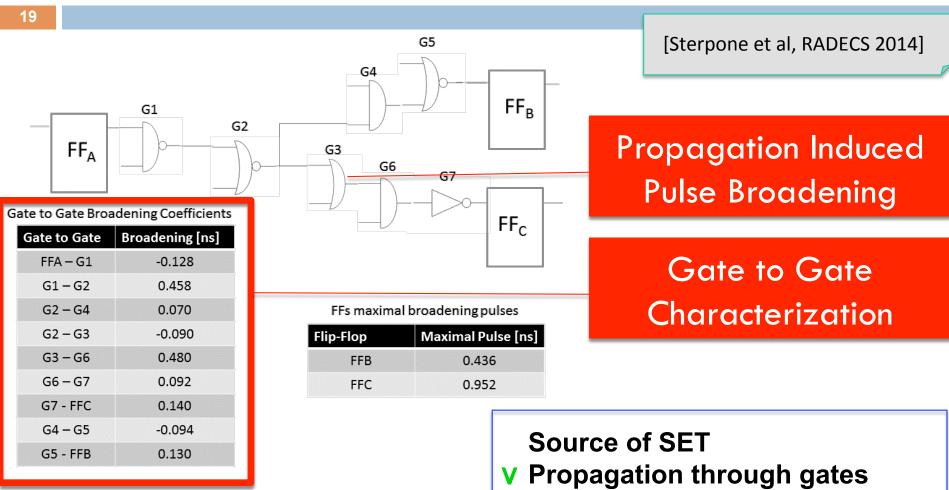
SET Propagation through routing



Propagation through routing

SET classification on FFs or IOs

SET Propagation through routing

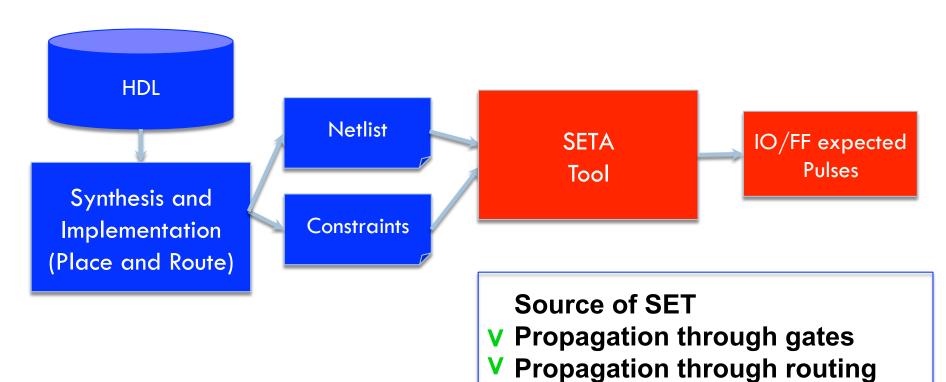


V Propagation through routing

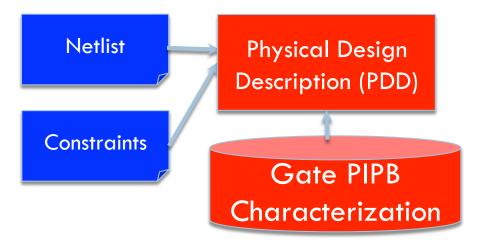
SET classification on FFs or IOs

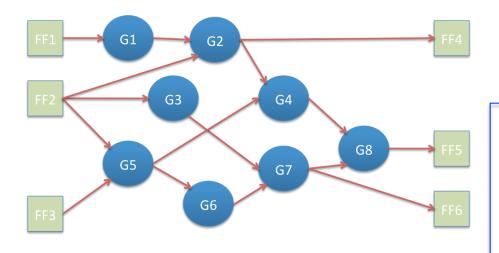
SET classification on FFs and IOs

- A tool has been developed:
 - Single Event Transient Analyzer (SETA)

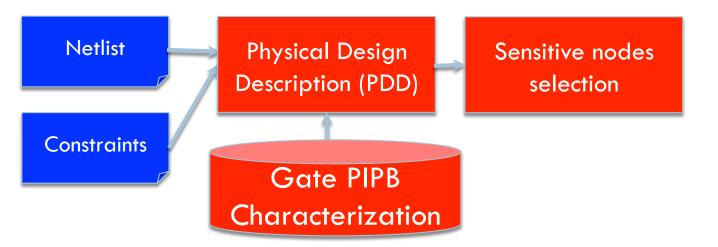


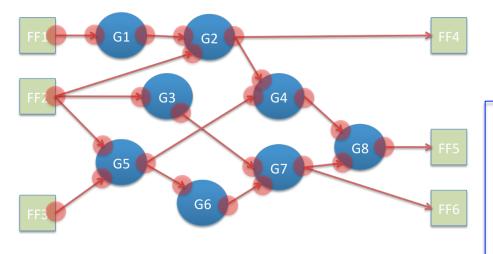
SET classification on FFs or IOs



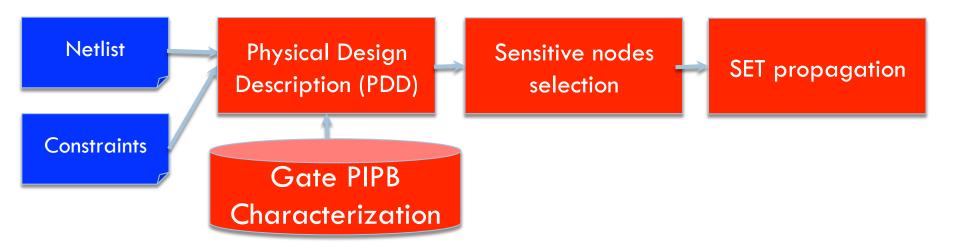


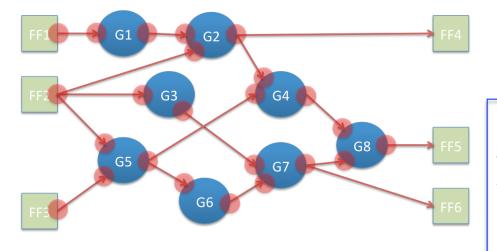
- V Propagation through gates
- Propagation through routingSET classification on FFs or IOs



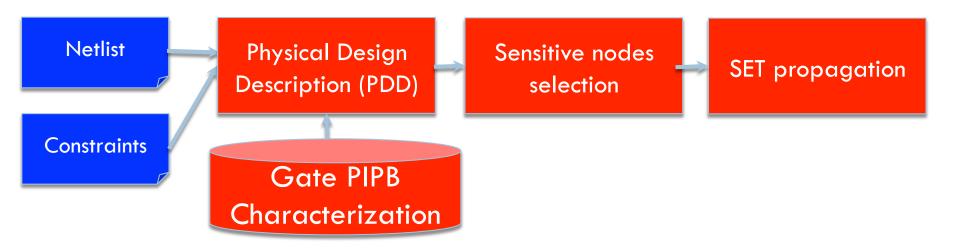


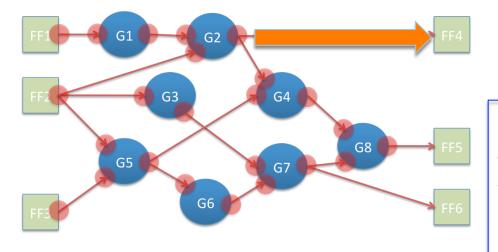
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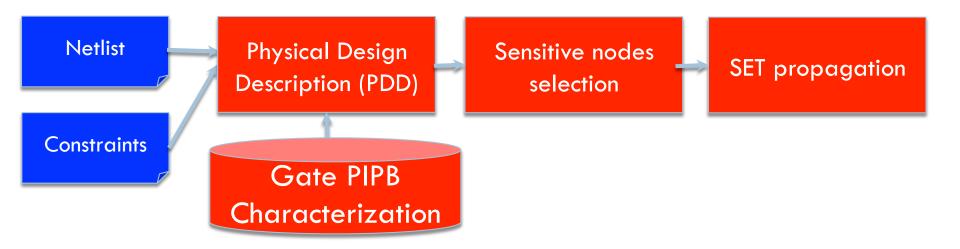


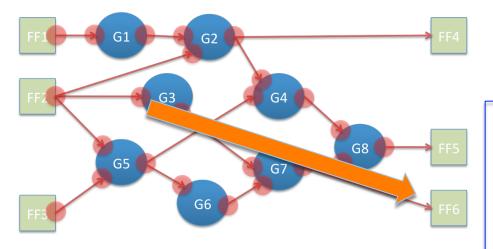
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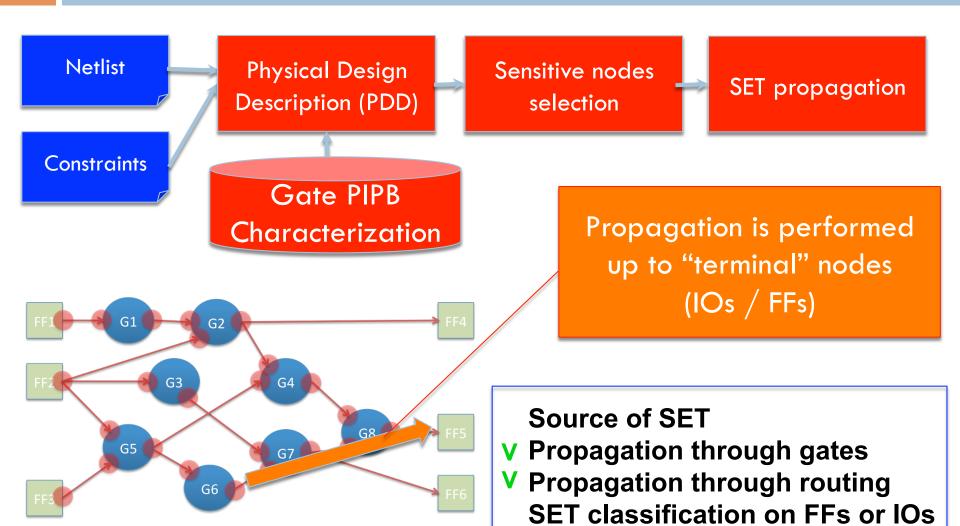


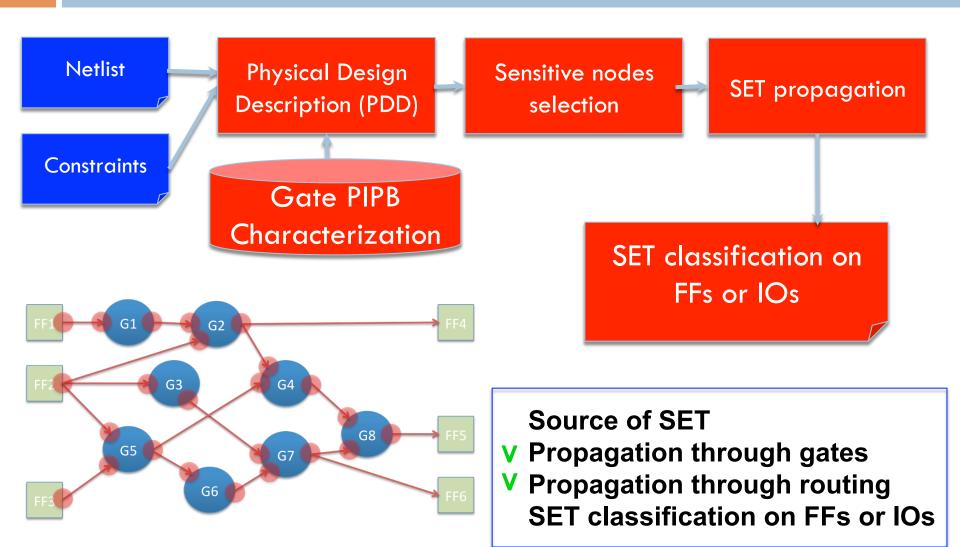
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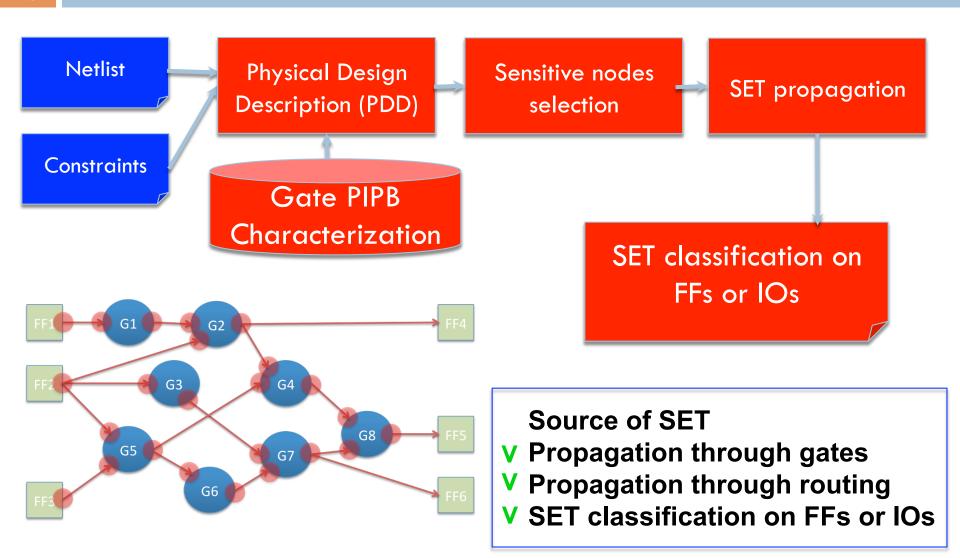




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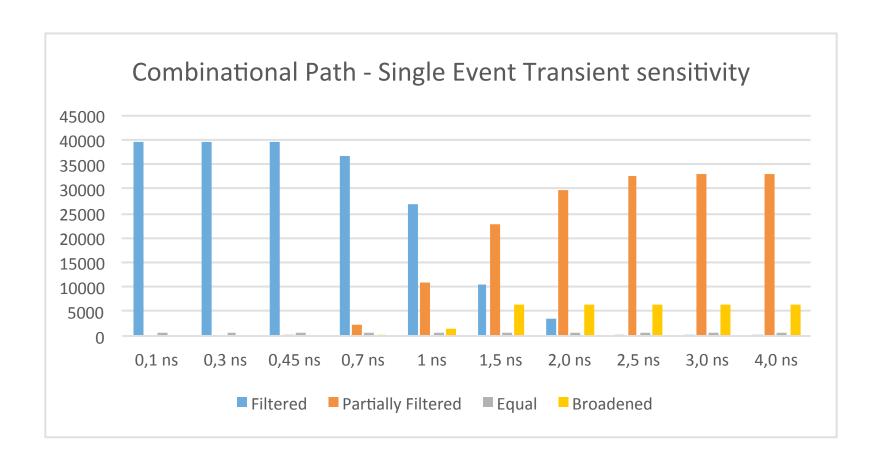




SET classification on FFs and IOs

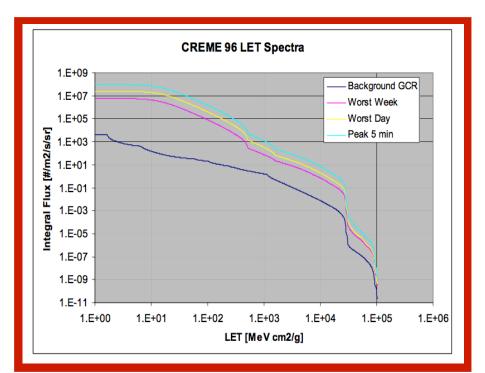
- The classification identifies the number of SET:
 - Totally filtered
 - Partially filtered
 - Equally propagated
 - Broadened

SETA results – EUCLID project



SETA results – EUCLID project

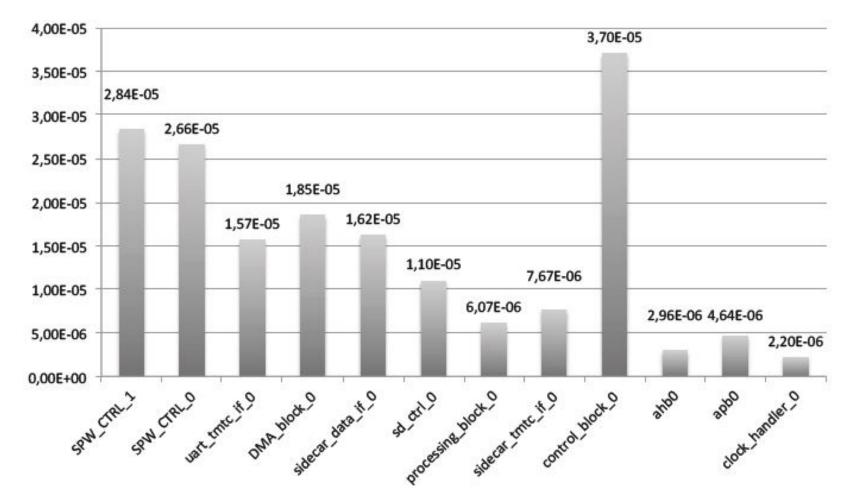
- → Analysis of the integral fluency expected for the duration of the mission: expected EUCLID duration is 6.25 years
 - Linear Energy Transfer distribution calculated using CREME96



Resource	SET Normalized cross-section	
Routing Segment	1.31E-10	
VersaTile	2.60E-08	

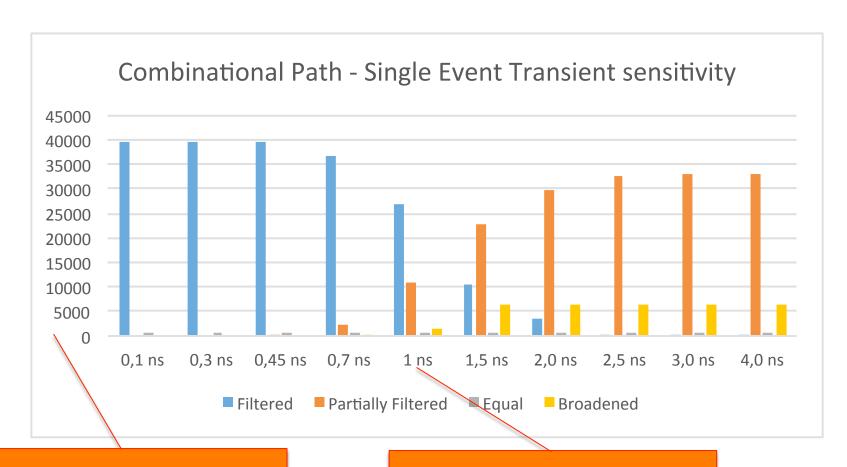
Transient Error cross-section per module

SETA results – EUCLID project



Circuit module

SETA results – EUCLID project



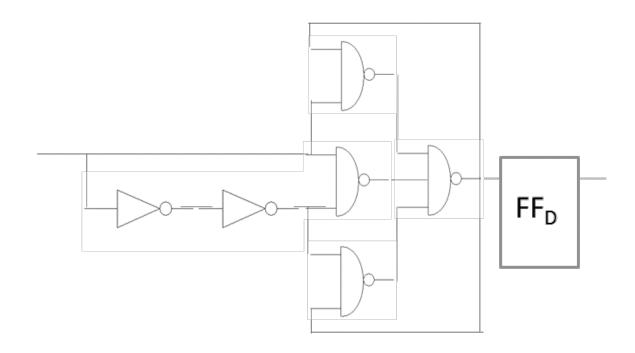
Total number of analyzed SET

Type of SET per injected pulse

SET: mitigation

[Sterpone and Du, IEEE ETS 2014]

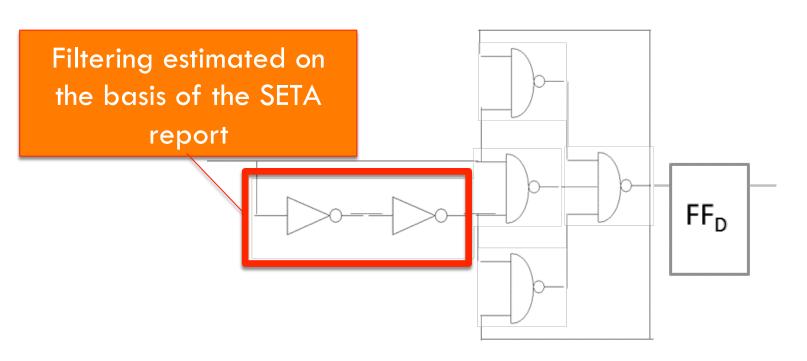
- Selective guard gate (GG) mapper
 - Inserting a GG logic structure in the input of the selected FF



SET: mitigation solution 1

[Sterpone and Du, IEEE ETS 2014]

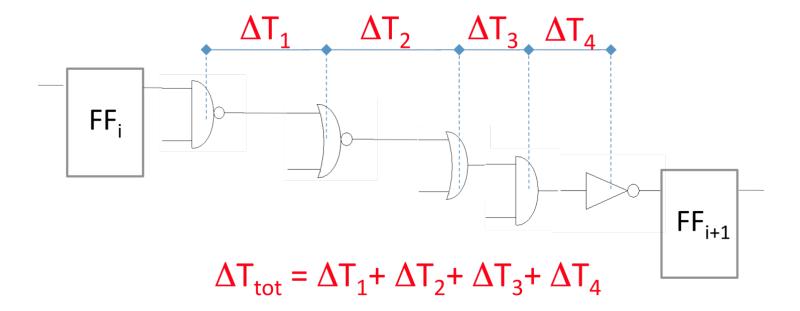
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SET: mitigation solution 2

[Sterpone and Du, IEEE ETS 2014]

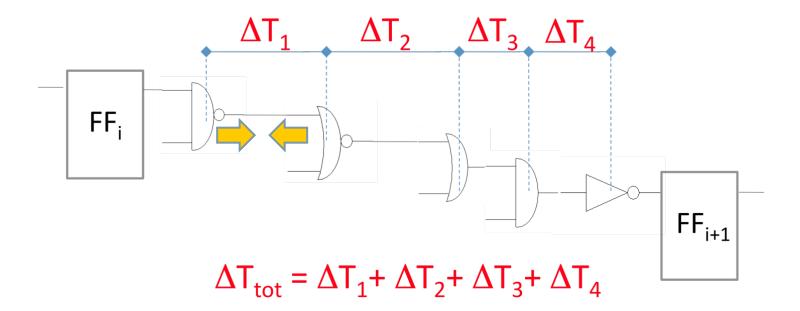
- Accurate placement acting on the critical paths
 - Distance between gates is modified in order to maximize the electrical filtering effect



SET: mitigation solution 2

[Sterpone and Du, IEEE ETS 2014]

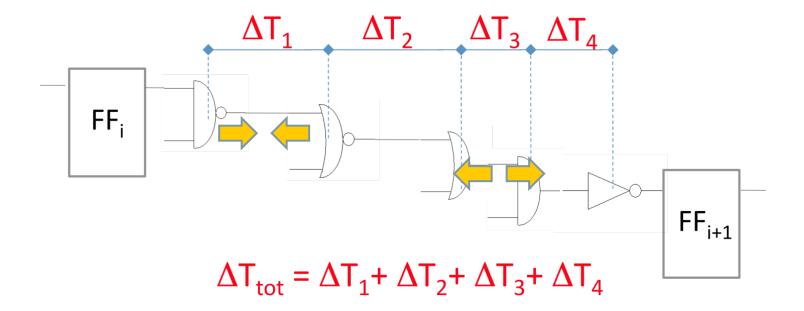
- Accurate placement acting on the critical paths
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SET: mitigation solution 2

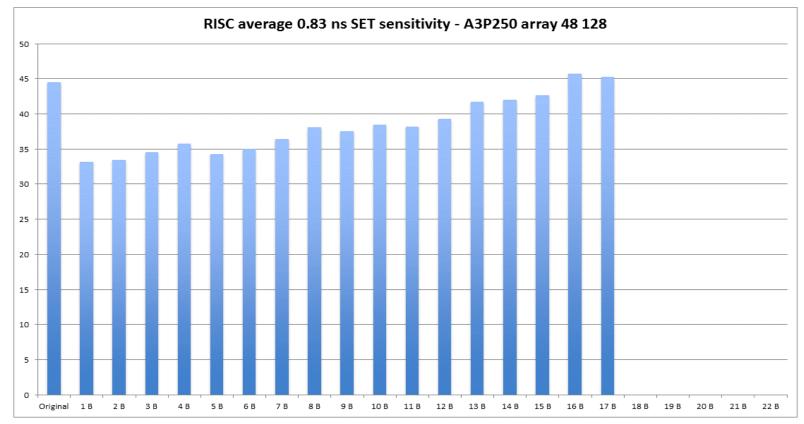
[Sterpone and Du, IEEE ETS 2014]

- Accurate placement acting on the critical paths
 - Distance between gates is modified in order to maximize the electrical filtering effect



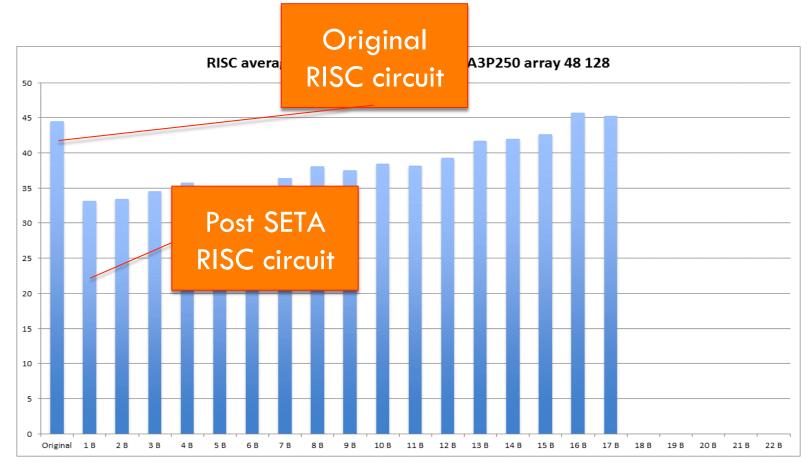
SET: mitigation results





Different place and route constraints

SET: mitigation results

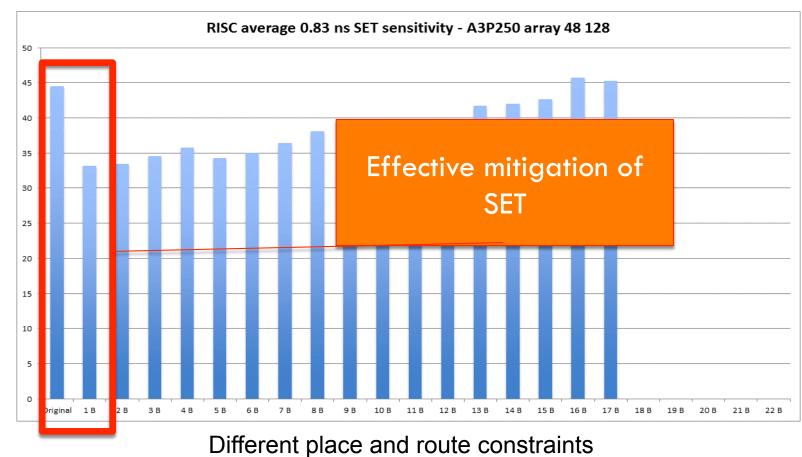


Average SET sensitivity

Different place and route constraints

SET: mitigation results





SET: mitigation radiation test results

- Heavy ions test performed at the Cyclotron of the Université Catholique de Louvain (UCL)
 - □ Kripton ion with a fluence of 3.04E8 (particles)
 - □ Average flux 1E4 (particles/sec)
 - □ RISC working frequency of 20MHz on ProASIC3 A3P250

RISC processor version	SEE Cross-section [MeV cm ² /mg]
Unhardened	1.45E-9
Full TMR + GG	6.37E-10
Our Approach	3.12E-12

- SETA tools are available
 - □ Effective analysis of SET propagation
 - Effective overall SET mitigation

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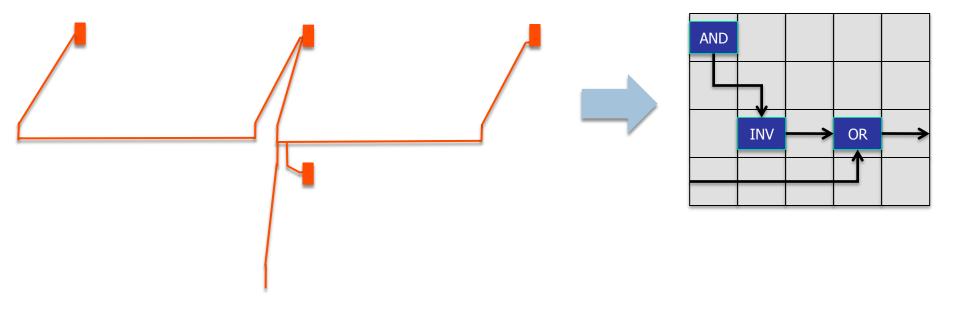
- SETA tools are available
 - Effective analysis of SET propagation
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- **X Source of SET**
- V Propagation through gates
- V Propagation through routing
- **V** SET classification on FFs or IOs

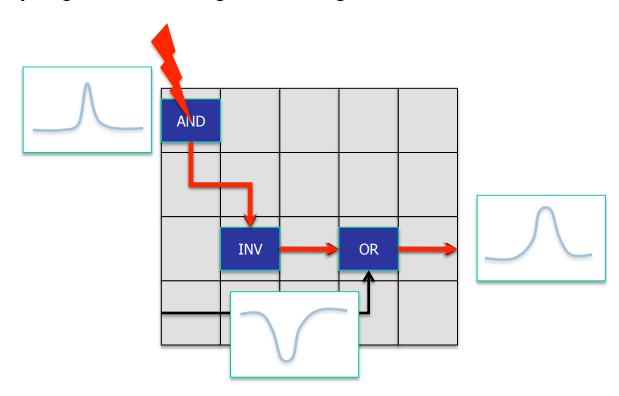
Physical Design Description

- □ The circuit is modeled as a graph
 - Cell functionality
 - Routing model



SET generation phenomena

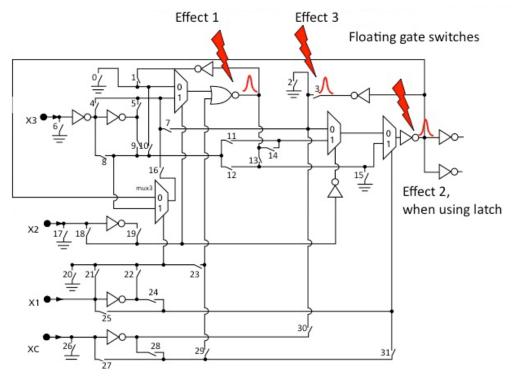
- Particle hitting a sensitive node
 - □ Generate a SET pulse
 - Propagates through the logic



SET generation phenomena

- SET generation is related to
 - Linear Energy Transfer (LET)
 - VersaTile architecture
 - Technology

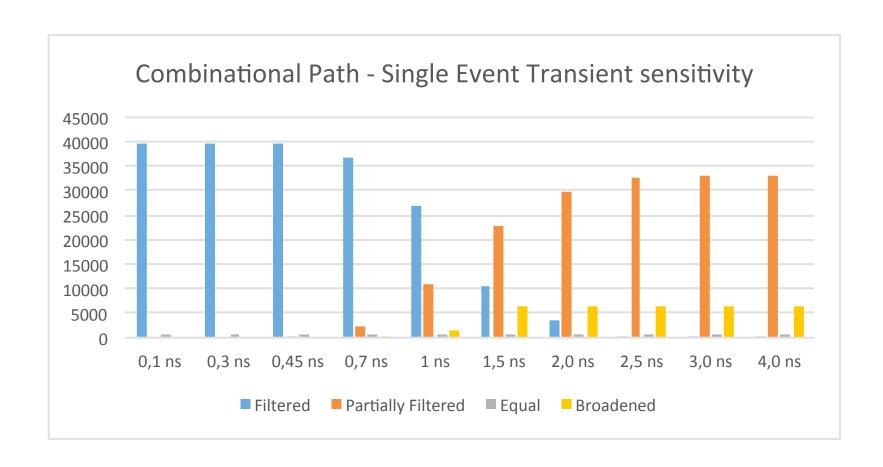
[Azimi, Du, Sterpone, Micro Rel, 2015] [Azimi and Sterpone, IEEE DDECS 2016]



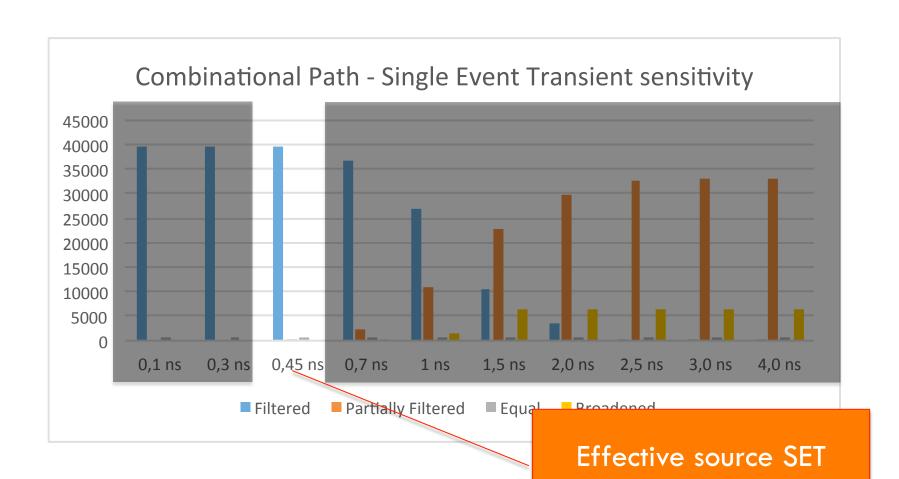
Why SET generation?

- The type of source SET is mandatory to understand the exact type of propagation
 - Mitigation GG insertion is related to SET length
- □ It is necessary to establish the absolute SET count
 - Calculation of the realistic IOs/FFs error rate for the whole space mission duration

Why SET generation?

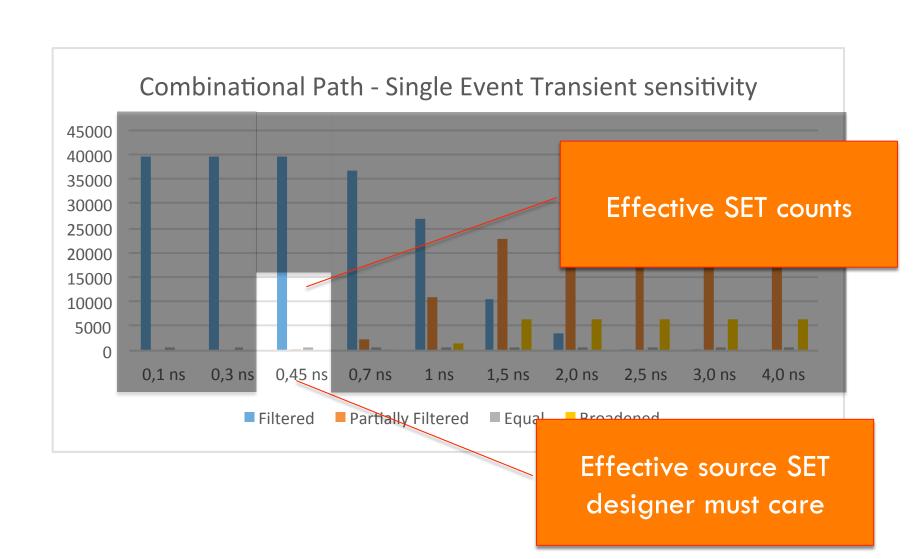


Identification of source SET length



designer must care

Identification of effective SET counts



Thank you!

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