Sanitas product 1q 2016 Architecture & Features

Sandro Pastore

MAY 2016

Sanitas EG: INAF spin off

- Research
  - Radiation effects on FPGA devices
- Industrial
  - Vision
  - Motor control
- Imaging
  - Surveillance camera & Industrial camera
  - FPGA analytics
  - Hi performance sensor
- Space and avionics
  - DO 254 development flow
  - FPGA based CPU board
  - Fault injection system
- Telecommunications
  - Ethernet QOS IP cores
- Production
  - Test and qualification process

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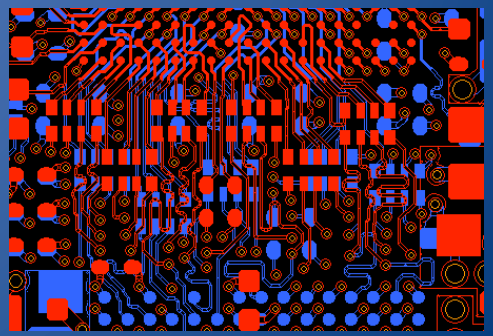
DIGITAL SYSTEMS, RESEARCH AND INNOVATION

2000
3 people

2005
5 people

2015
11 people

INAF



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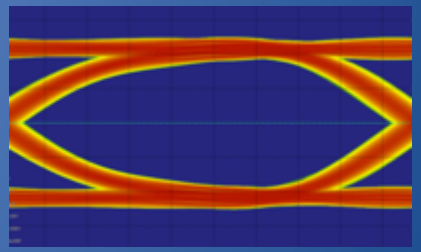
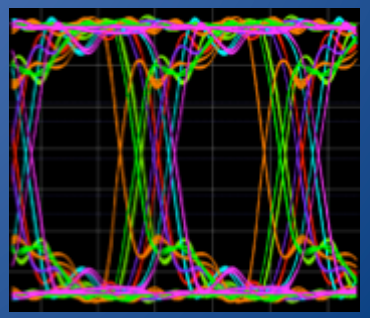
Sanitas Expertize

- Complex system design
  - Data driven
  - Hardware/software co-design
  - Design for testability
  - Qualified design (space, avionics)
- HI End hardware development
  - Multi gigabit serial interface
  - High Performance Analog interfaces
  - FULL SPEED DDR memory interfaces
- FPGA experiences, Xilinx and Lattice tool chains





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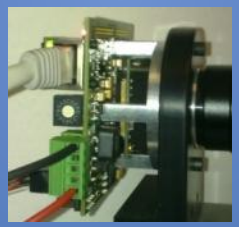
Some success stories:

- SKA radiotelescope digitalizer, 32 GByte/sec, 40G Ethernet

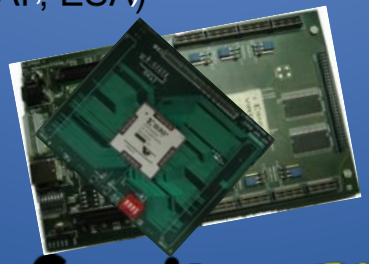
- HI REL SBC with 1GHz PPC for space application (ESA, Thales)

- 10 GBit FPGA Ethernet Board for QoS and IDS

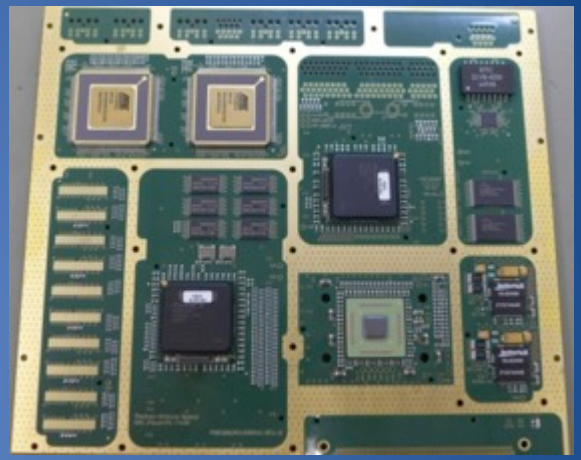
- CCD camera for industrial applications



- System for SEU fault emulation in SRAM FPGAs (INAF, ESA)



- METEOSAT - ESA satellite



- FPGA based industrial cameras

Sanitas portfolio

- NEW Hardware
  - High performance data acquisition, Xilinx Ultrascale
    - SKA Tile Processor analog acquisition board
  - NEW ECP5 camera platforms:
    - Inventami, SinC, SincGrab

All internally developed

- Intellectual Propriety
  - FPGA IP cores (Video Pipeline, DDR multiport, UDP video streamer, video motion, encryption IP core, various bus interfaces)

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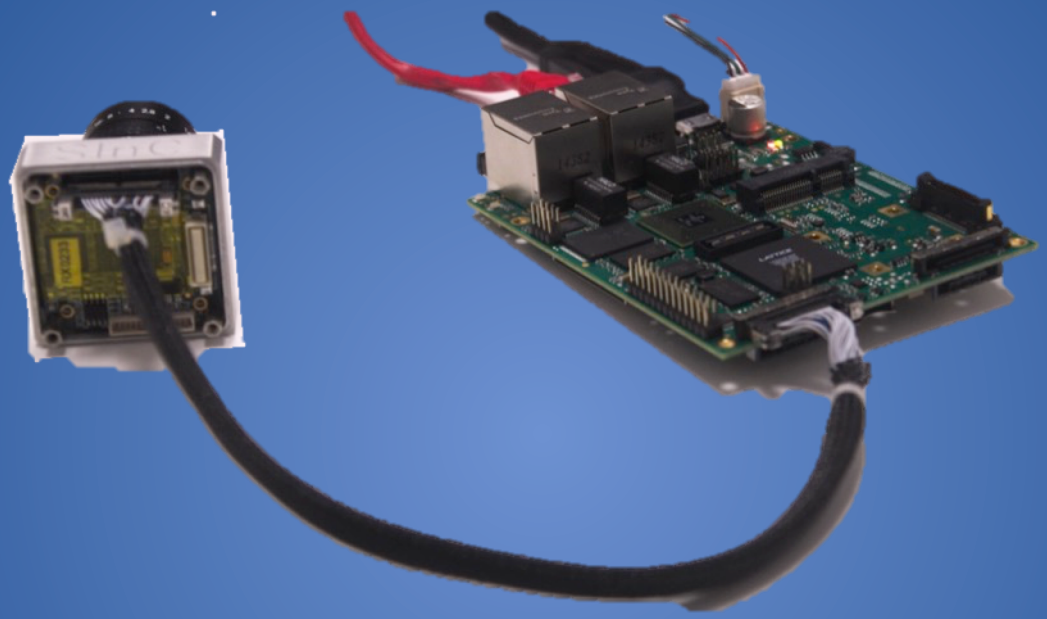

CAMERA PLATFORMS

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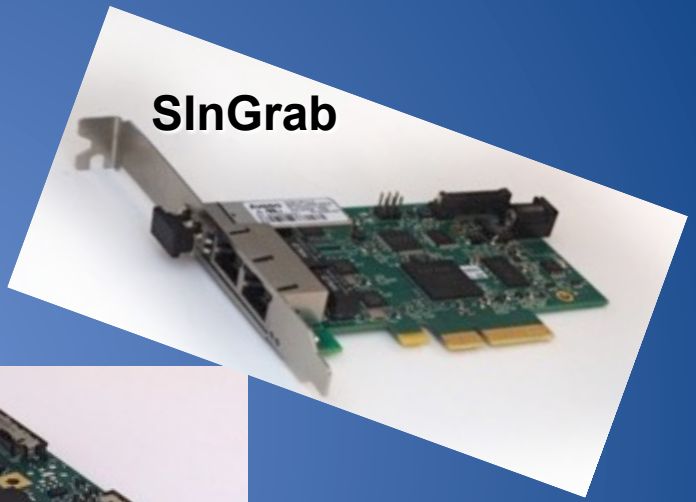
New Sanitas 2015 ECP5 Bard



IP & Driver

Thinking for rapid prototyping and production of High End application

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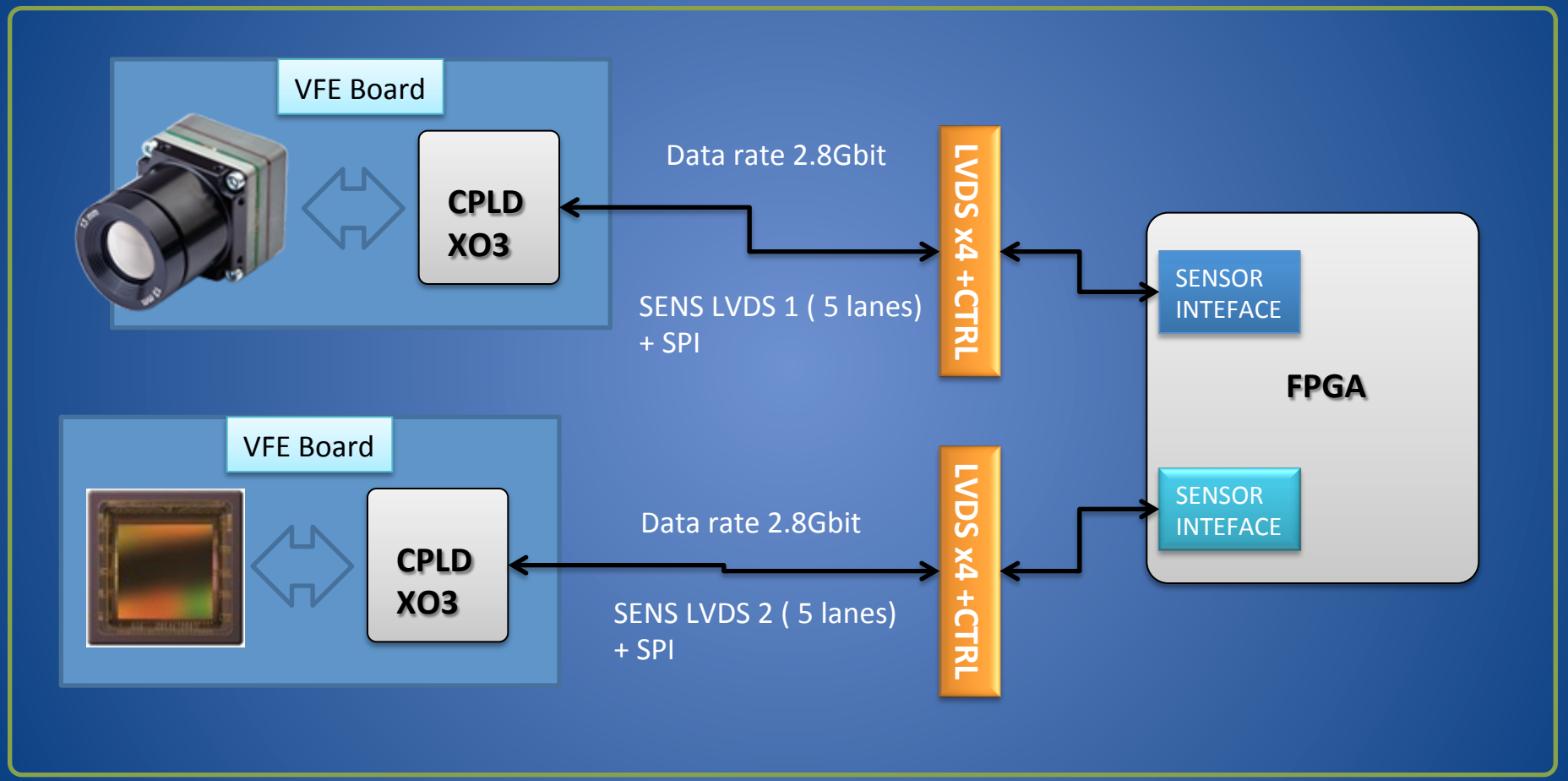
Sensor board: standardized IF



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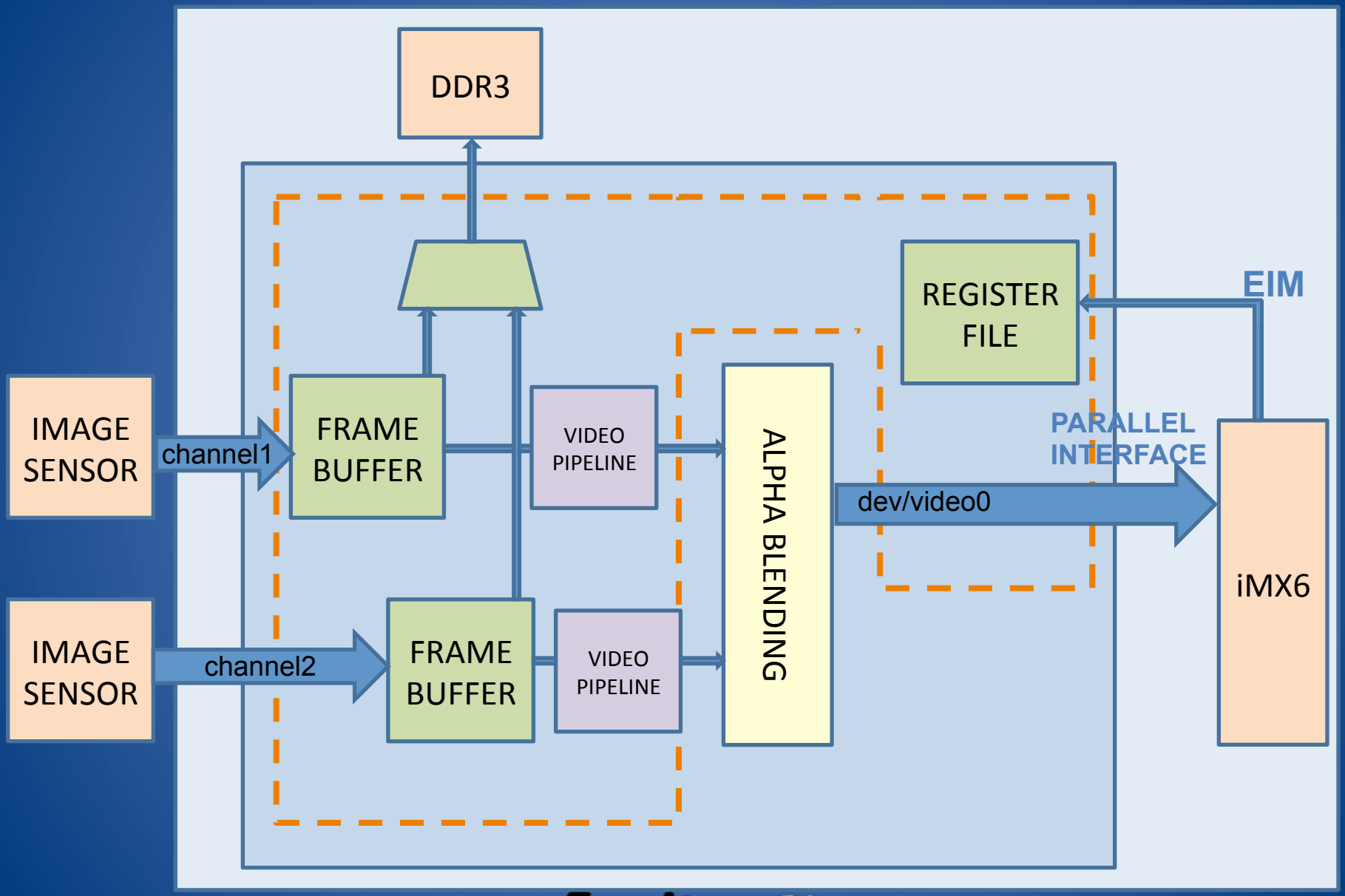
INVENTAMI

FPGA Customizable Architecture



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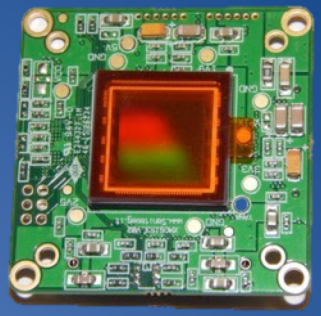
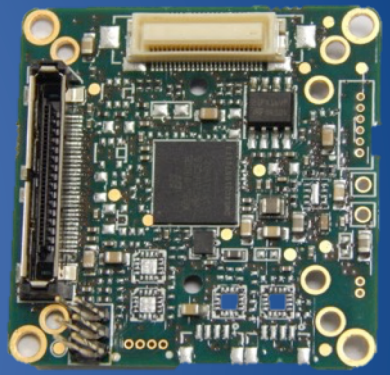
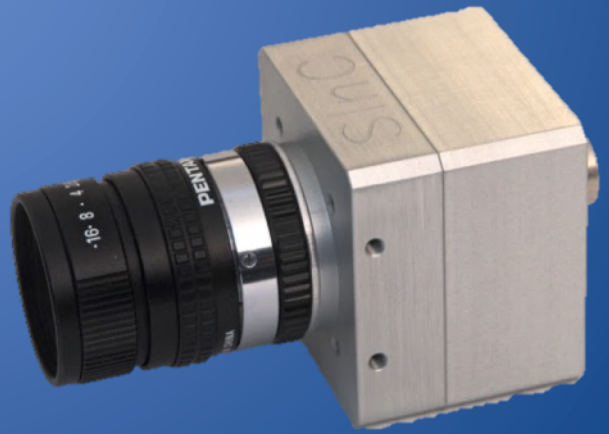
SInC Industria Camera







- ✓CMOSIS CMV4000 / CMV2000 Rev3
- ✓CMOS 2 MP or 4 MP sensor with electronic global shutter
- ✓Colour, monochrome or NIR CMOS
- ✓sensor with 1” optical format
- ✓Resolution of 2048 x 2048 using 5.5x5.5 µm2 pixels
- ✓30 fps at full resolution (4 MP)
- ✓1000BASE-T Ethernet IF
- ✓45 x 45 x 37 mm with 8 mounting points
- ✓ 8 configurable GPIOs
- ✓256 MB DDR3 frame buffer (up 1 GB)
- ✓Region Of Interest (ROI)

- ✓Version with 5Mpixel APTINA

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INVENTAMI

INVENTAMI

SINGLE BOARD COMPUTER

WWW.INVENTAMI.COM

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Inventami Extends i.MX6 capabilities

i.MX6 provides high-end features:

- Dual ARM Cortex A9 Core
- HW Graphics accelerators
- 1080p30 Enc/Dec Video Codecs
- ASRC Audio
- Image Processing Unit
- Display&Camera Interfaces
- Connectivity
- System Control
- Power Management
- ROM&RAM Internal Memories
- Security Control

+

INVENTAMI makes the difference:

- 4 HIGH-speed I/O interfaces
- 512 MByte dedicated DDR3-800
- FPGA 85K logic resources for hardware acceleration
- Additional Gigabit Ethernet (full bandwidth)
- 3 HIGH-speed interfaces to i.MX6

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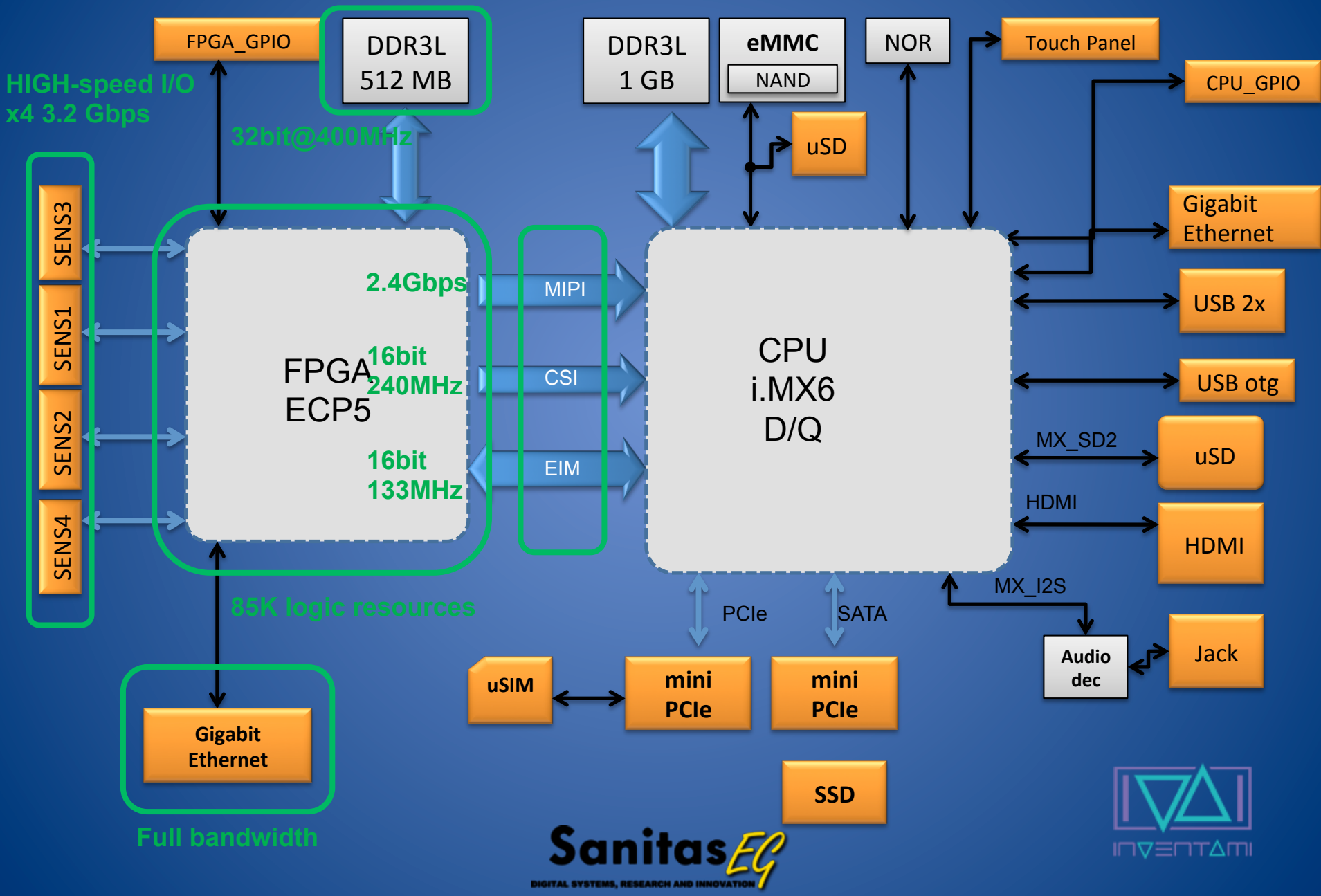
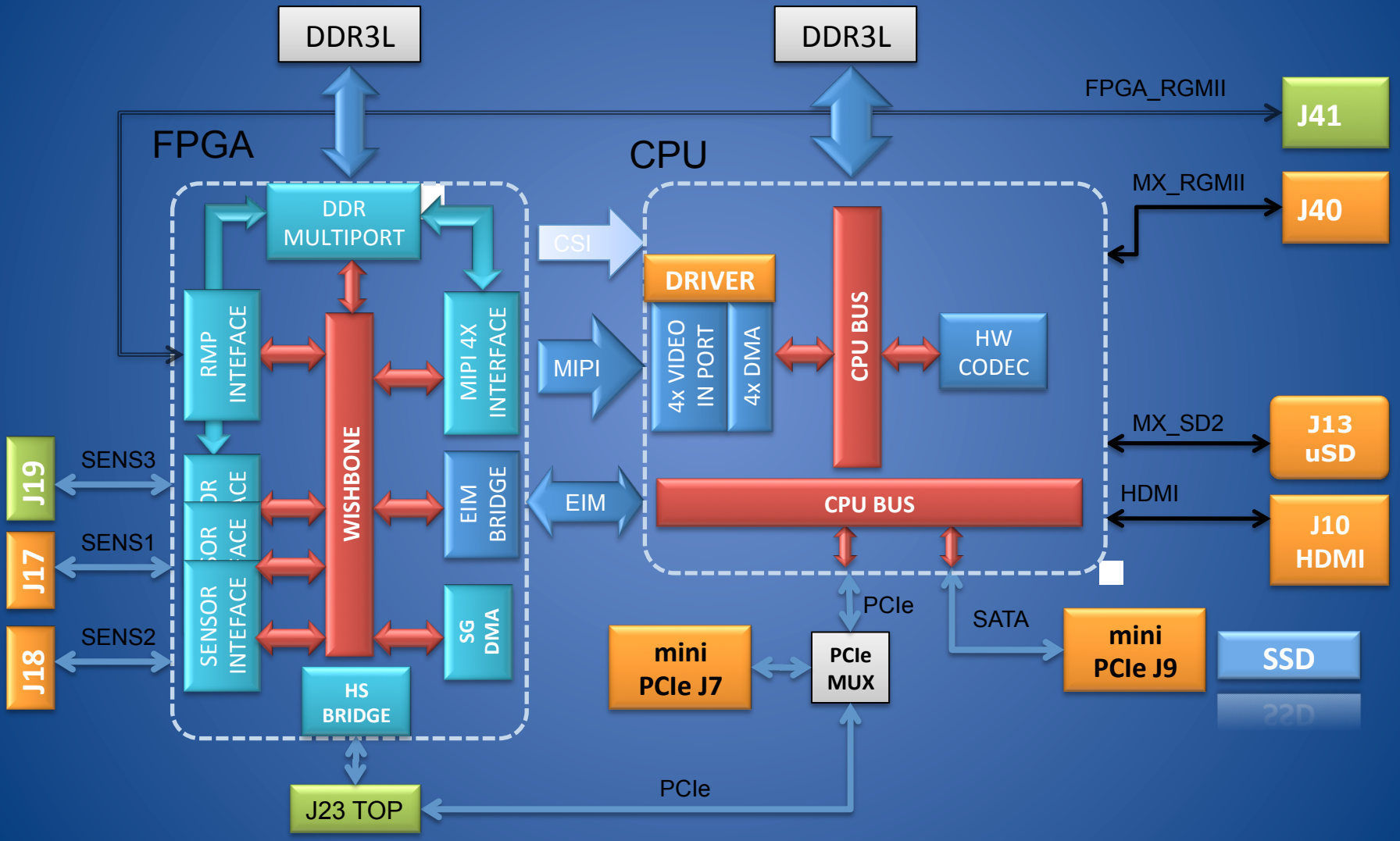
INVENTAMI

Inventami Block Diagram



Four Channel concept on Inventami



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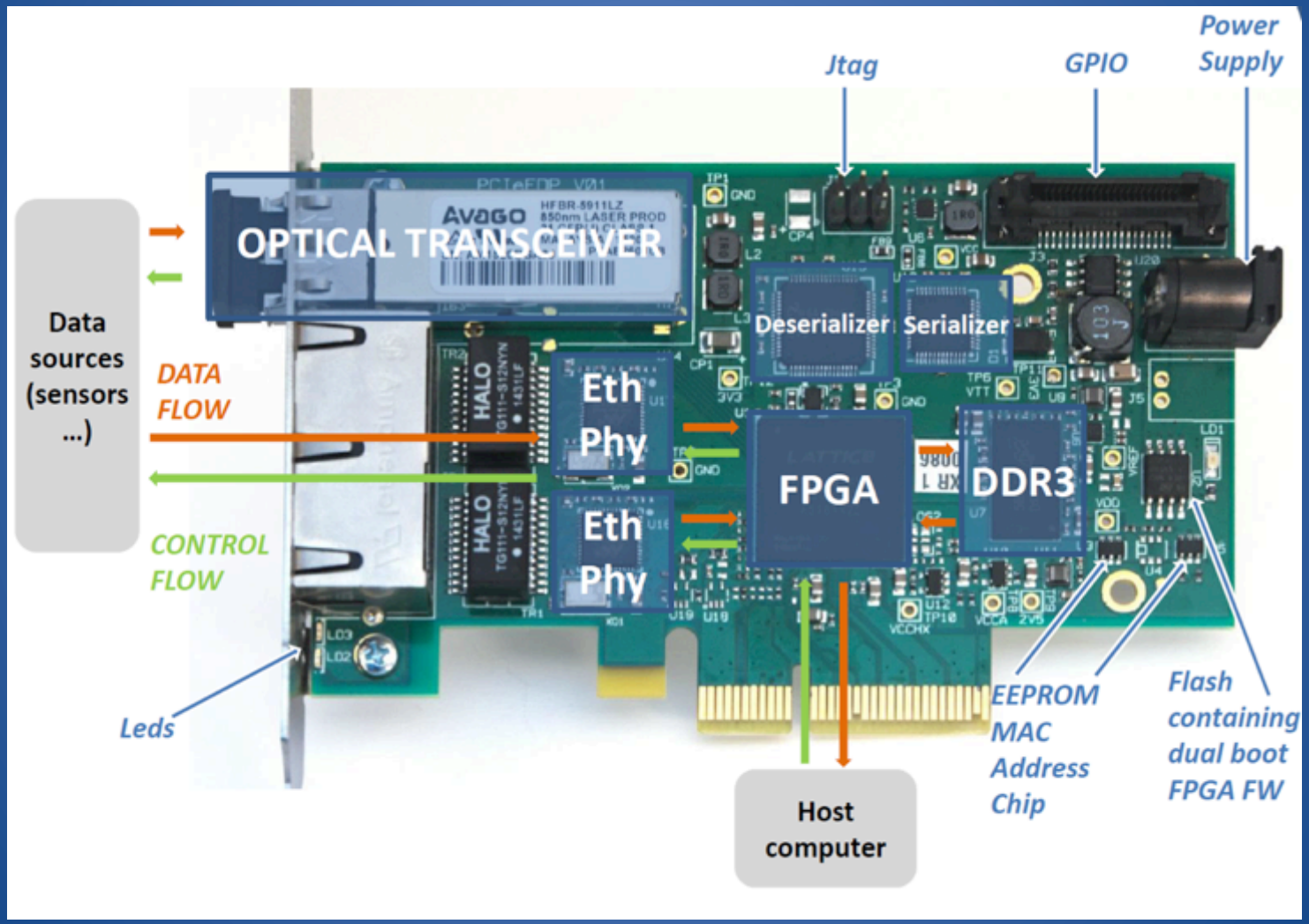
SInGrab Board



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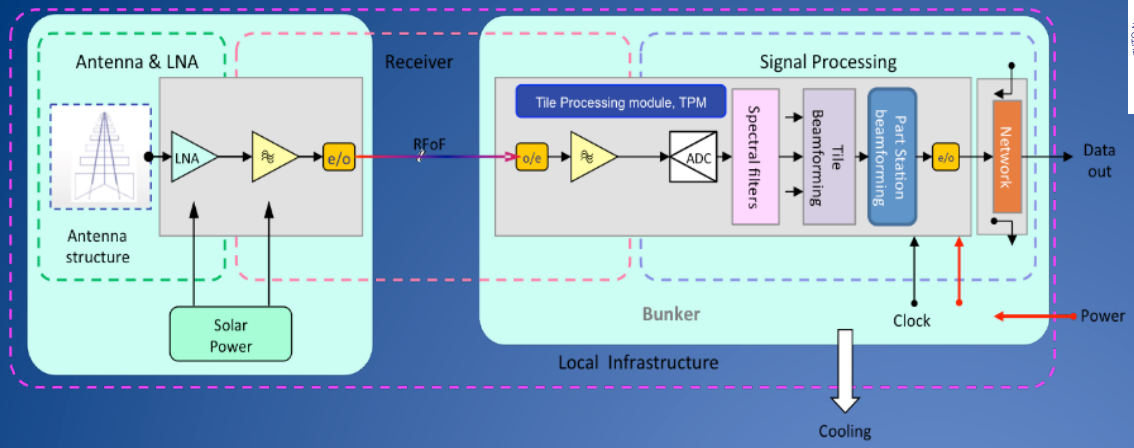

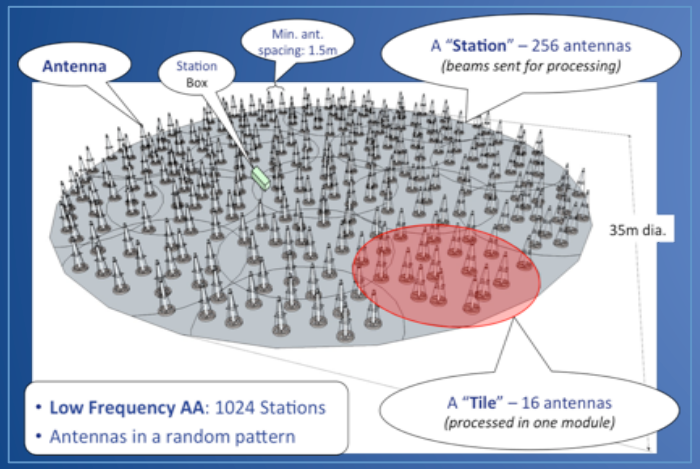

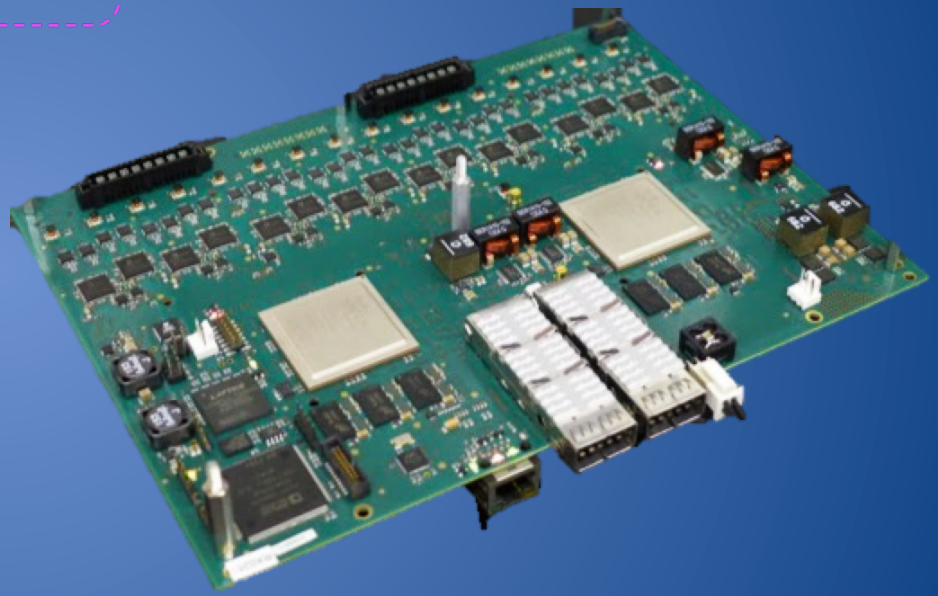

ITPM: SIGNAL PROCESSING BOARD FOR SKA

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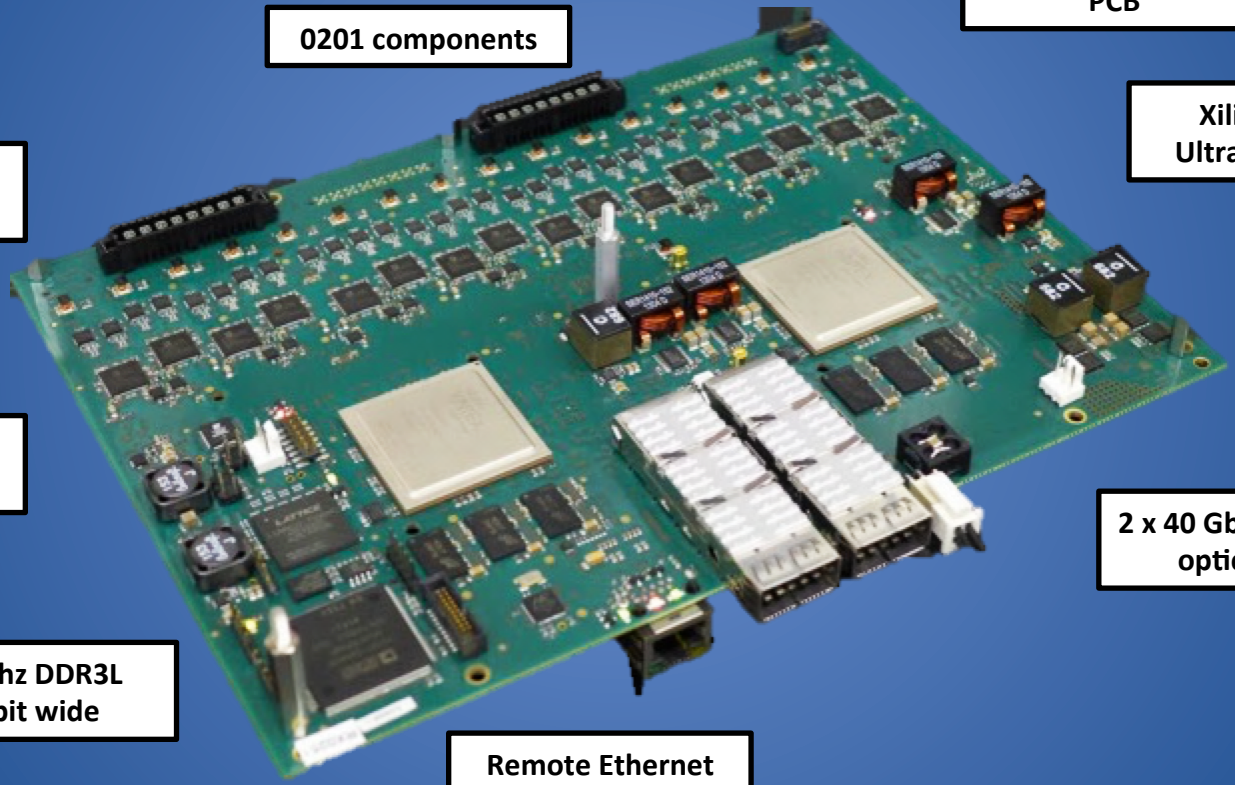
iTPM Technologies



Multimaterial RF PCB

0201 components

Xilinx 20 nm Ultrascale FPGA

32 channel AD 14 bit @ 1 GHz

16 x 10 Gbit AD JESD lines

2 x 40 Gbit Ethernet optical link

1.6 Ghz DDR3L 96 bit wide

Remote Ethernet management

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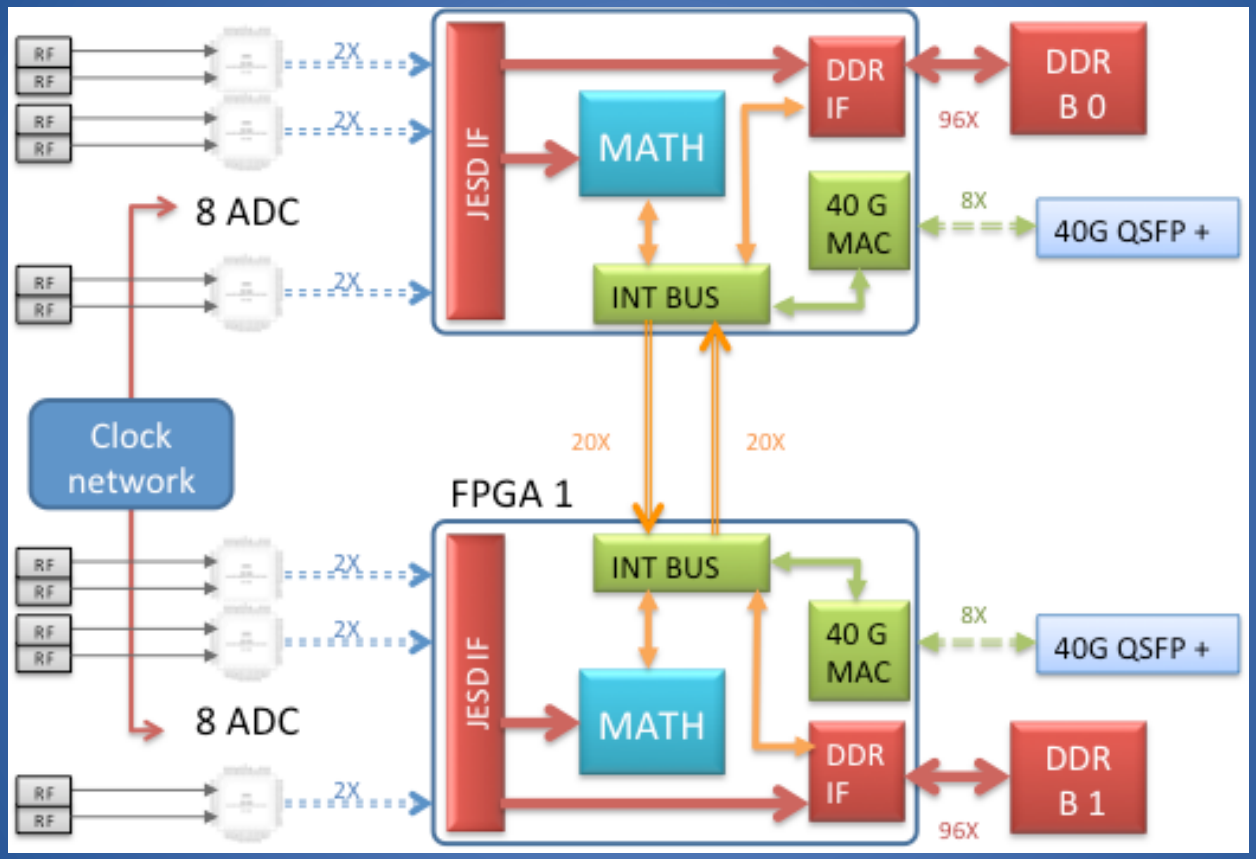
Acquisition and processing architecture



FPGA USAGE:	JESD RX	INT BUS	DDR	40G Eth
	16 GByte/s	5.0 GByte/s	16 GByte/s	5.0 GByte/s

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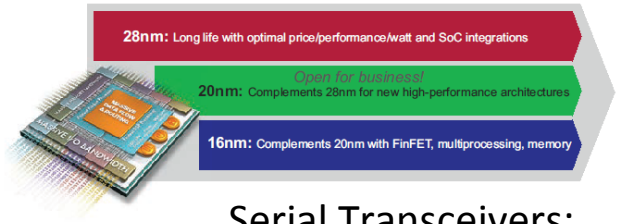
FPGA Xilinx Ultrascale U40, 20 nm

Part Number	XCKU040	XCKU060	XCKU075
Logic Cells	424,200	580,440	756,000
CLB Flip-Flops	484,800	663,360	864,000
CLB LUTs	242,400	331,680	432,000
Maximum Distributed RAM (Kb)	7,050	9,180	7,290
Block RAM/FIFO w/ECC (36 Kb each)	600	1,080	1,188
Block RAM/FIFO (18 Kb each)	1,200	2,160	2,376
Total Block RAM (Mb)	21.1	38.0	41.8
DSP Slices	1,920	2,760	2,592



Production
1q 2015

Serial Transceivers:

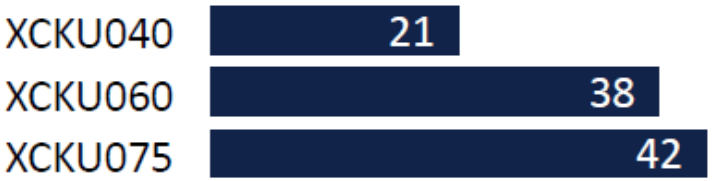
XCKU040 20

GTH = 16.3 Gb/s

DSP Slice Count

Speed grade	-1	-2	-3
F_{MAX} [MHz]	594	661	741
Max GMAC/s	6558	7297	8181

Block RAM Capacity (Mb):



Speed grade	-1	-2	-3
True dual-port Block RAM F_{MAX} [MHz]	525	585	660

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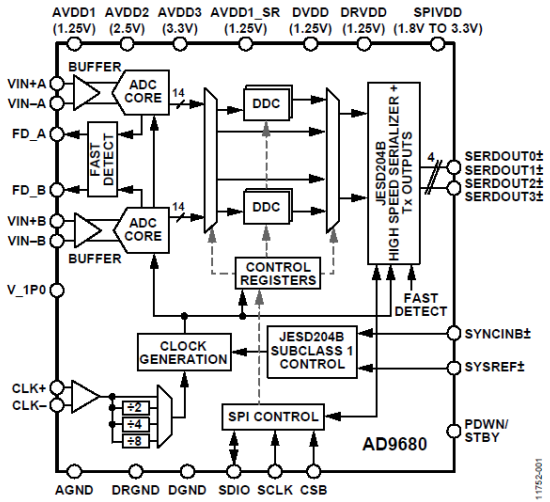
ADC 14 bit @ 1 GHz, AD9680

FEATURES

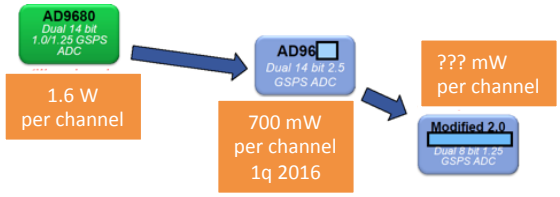
JESD204B (Subclass 1) coded serial digital outputs
1.65 W total power per channel at 1 GSPS (default settings)
SFDR = 85 dBFS at 340 MHz, 80 dBFS at 1 GHz
SNR = 65.3 dBFS at 340 MHz (A_{IN} = −1.0 dBFS),
61.4 dBFS at 1 GHz
ENOB = 10.8 bits at 10 MHz
DNL = ±0.5 LSB
INL = ±2.5 LSB
Noise density = −154 dBFS/Hz at 1 GSPS
1.25 V, 2.5 V, and 3.3 V dc supply operation
No missing codes
Internal ADC voltage reference
Flexible input range and termination impedance
1.46 V p-p to 1.94 V p-p (1.70 V p-p nominal)
400 Ω, 200 Ω, 100 Ω, and 50 Ω differential
2 GHz usable analog input full power bandwidth
95 dB channel isolation/crosstalk
Amplitude detect bits for efficient AGC implementation
2 integrated wideband digital processors per channel
12-bit NCO, up to 4 cascaded half-band filters
Differential clock input
Integer clock divide by −1, 2, 4, or 8
Flexible JESD204B lane configurations
Small signal dither

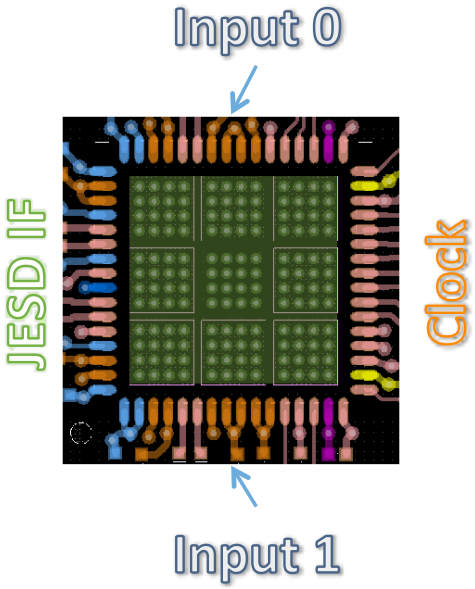
ANALOG DEVICES



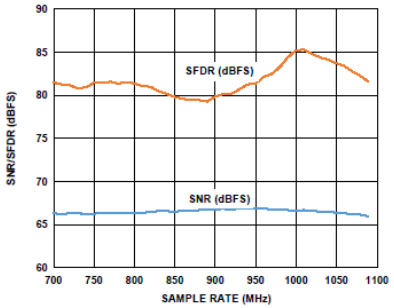
Roadmap to Lower Power

(Power Estimates in SKA Configuration)





TYPICAL PERFORMANCE CHARACTERISTICS



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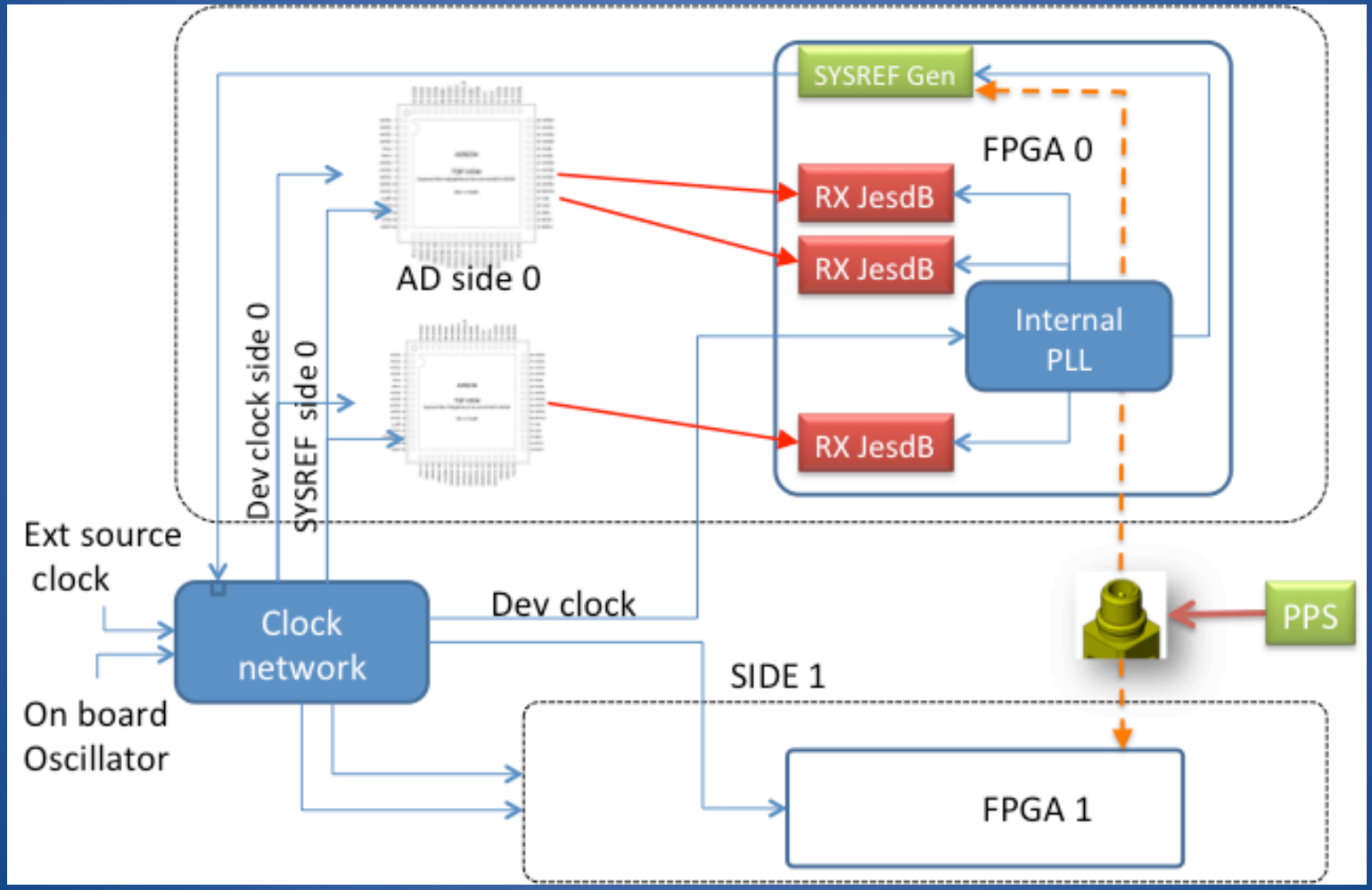
Data synchronization JESD204B, sub1



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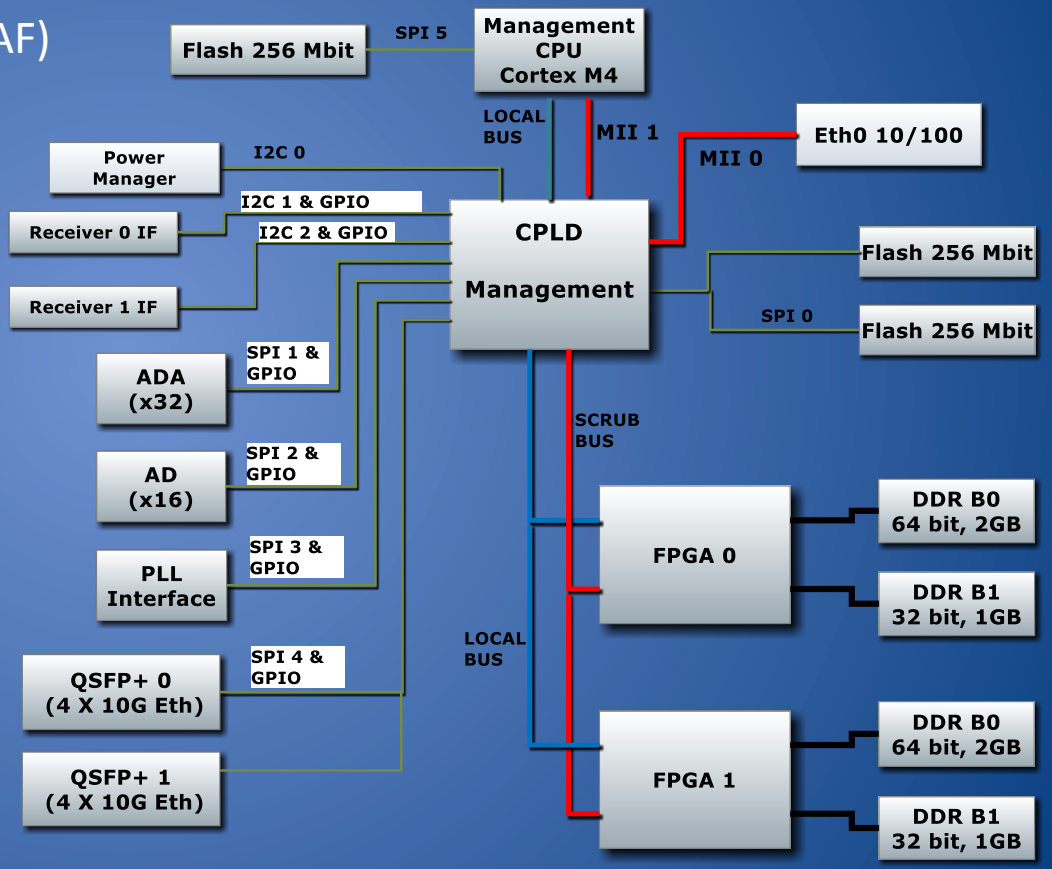
ITPM Management

- Cortex M4 CPU (ADSP-CM407BSWZ-AF)
  - Internal RAM (312 KB) & FLASH (2 MB)
  - Ethernet IF with CPLD
- Management CPLD
  - Ethernet switch and UDP-RMP core
  - FPGA Select MAP IF
  - CPU Local BUS IF
  - CONTROL & STATUS REGS (GPIOs)
  - SPI IF
  - I2C IF
  - FPGAs Local bus



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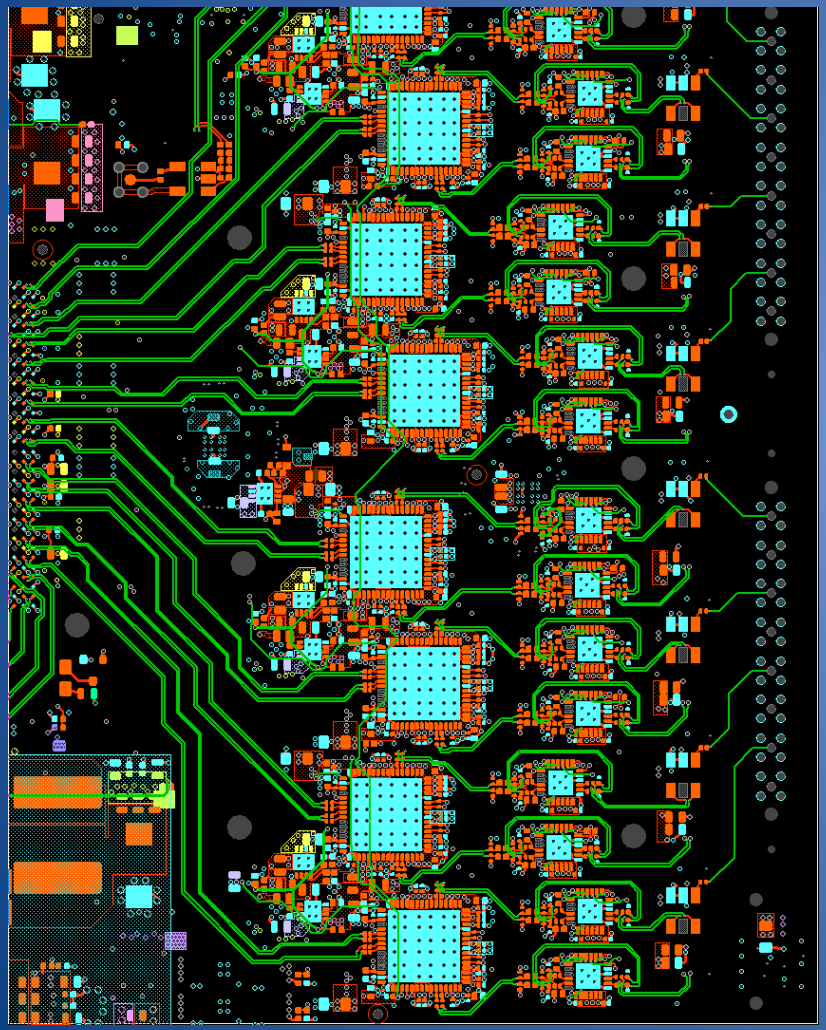
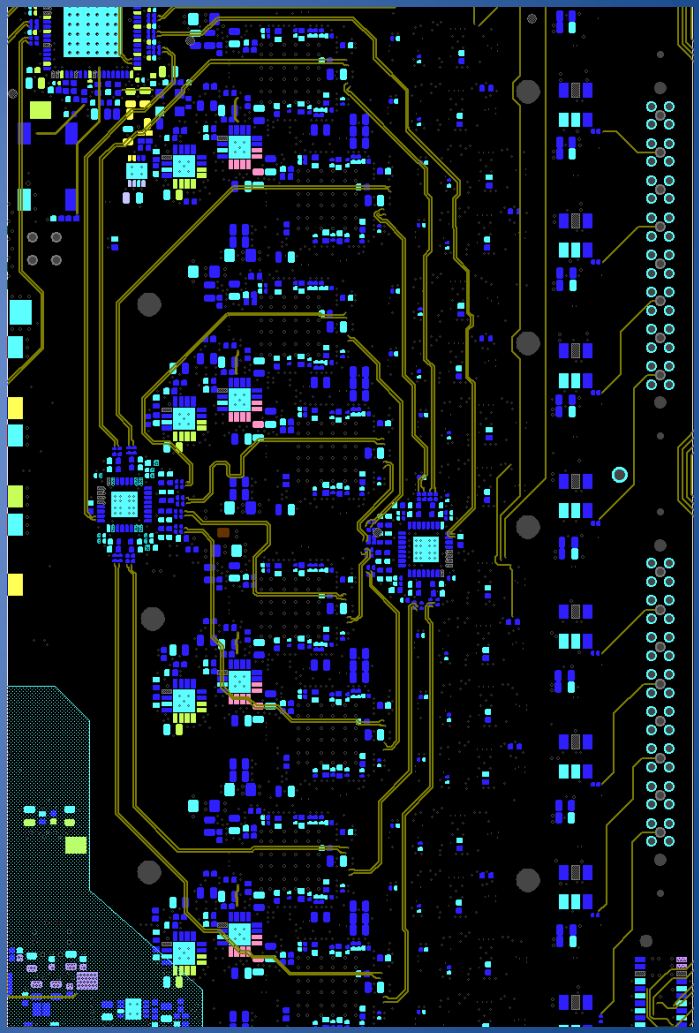
Layout topics





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ITPM RF PERFORMANCE

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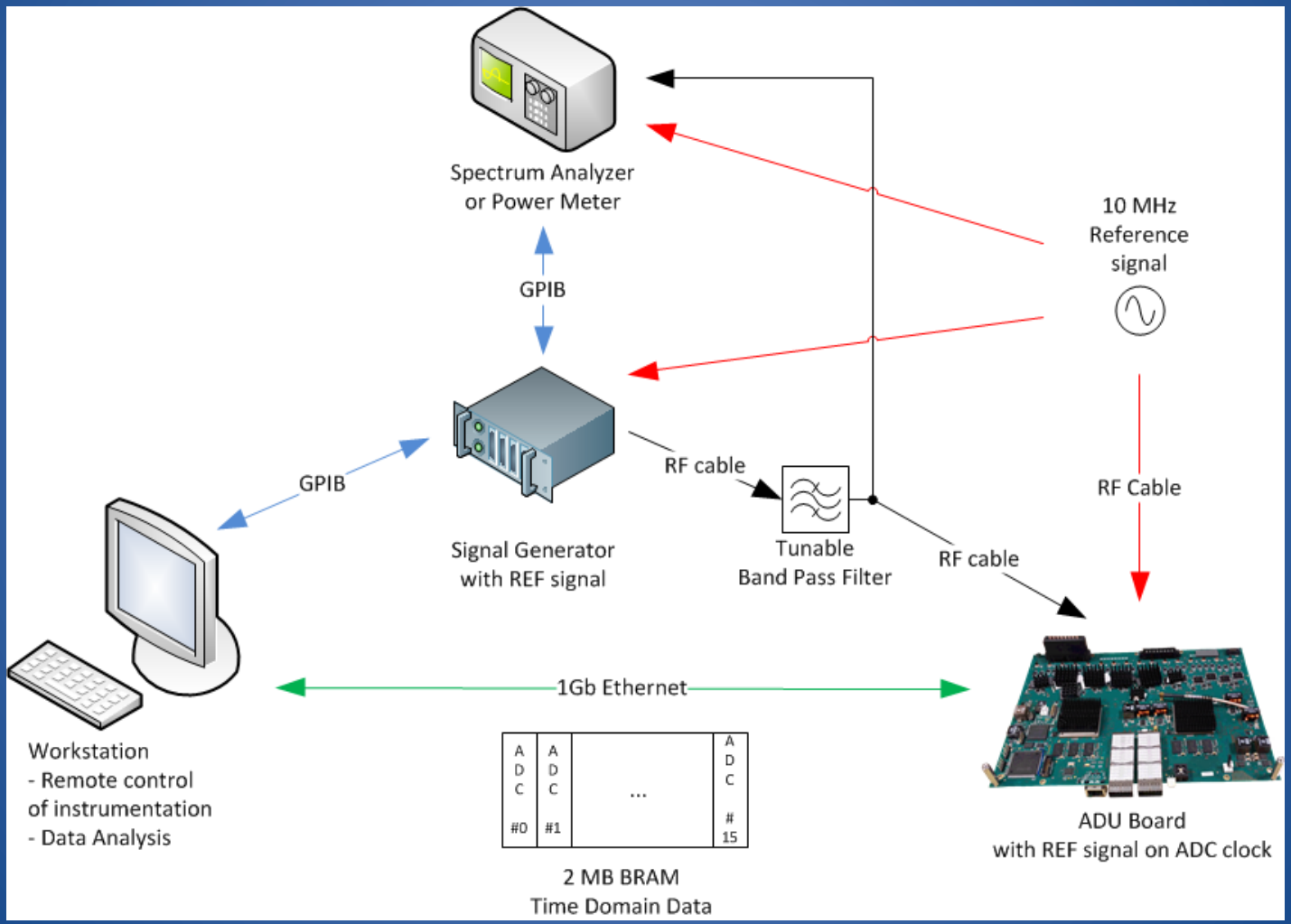
ADU Board Test Setup



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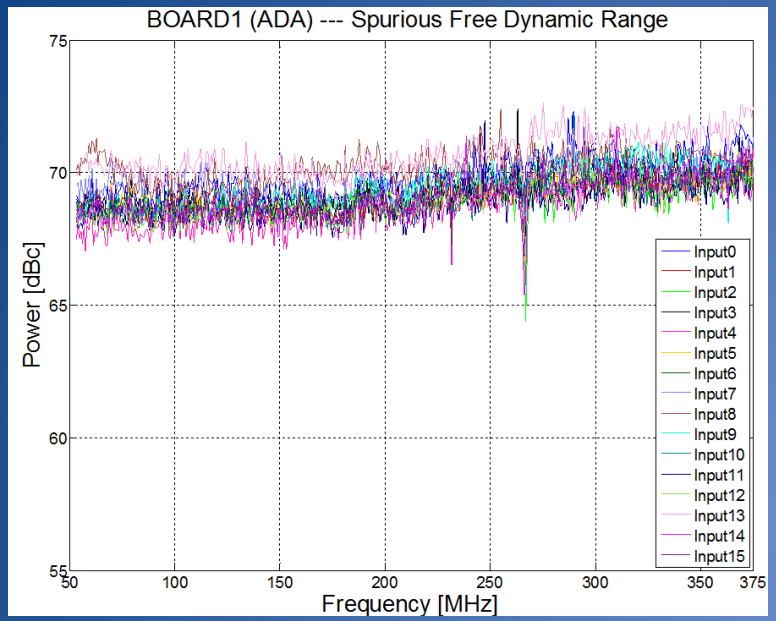
Measurement Summary

Fs: 800 MSPS --- BW: 50 – 375 MHz		
ADC Performance Parameters	**ADU Board#1 (with ADA)**	**ADU Board#2 (without ADA)**
Signal to Noise Ratio referenced to Full Scale [dBFS]	≥ 49.19	**≥ 49.33**
Gain Flatness [dBFS]	≤ ±0.3573	**≤ ±0.343**
2nd-order Harmonic Distortion [dBc]	≤ -67.24	**≤ -67.74**
3rd-order Harmonic Distortion [dBc]	≤ -66.53	**≤ -68.56**
Worst Other Spur [dBc]	**≤ -67.03**	≤ -66.83
Spurious Free Dynamic Range [dBc]	≥ 66.53	**≥ 66.83**
ENOB [bits]	≥ 7.876	**≥ 7.896**
Cross-Talk [dBc]	**≤ -65.69**	≤ -61
IP3 [dB] (F1=184.7 MHz; F2=187.5 MHz)	29.55	**32.2**
IP2 [dB] (F1=184.7 MHz; F2=187.5 MHz)	66.3	**77.5**

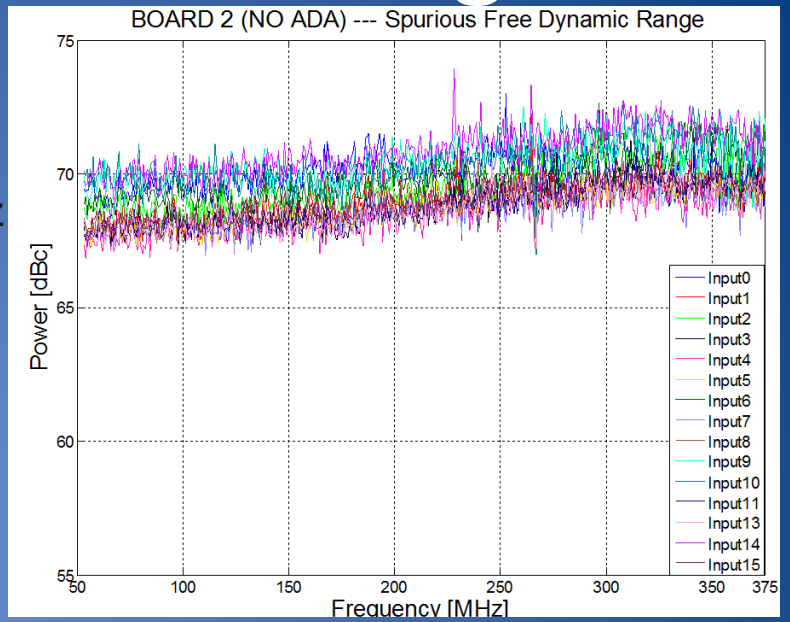
Fs: 700 MSPS --- BW: 375 – 650 MHz		
ADC Performance Parameters	**ADU Board#1 (with ADA)**	**ADU Board#2 (without ADA)**
Signal to Noise Ratio referenced to Full Scale [dBFS]	≥ 48.88	**≥ 49.32**
Gain Flatness [dBFS]	**≤ ±0.6252**	≤ ±1.356
2nd-order Harmonic Distortion [dBc]	**≤ -65.77**	≤ -59.9
3rd-order Harmonic Distortion [dBc]	≤ -60.78	**≤ -65.64**
Worst Other Spur [dBc]	**≤ -64.16**	≤ -63.23
Spurious Free Dynamic Range [dBc]	**≥ 60.78**	≥ 59.9
ENOB [bits]	≥ 7.788	**≥ 7.886**
Cross-Talk [dBc]	**≤ -70.58**	≤ -70.39
IP3 [dB] (F1=500.1 MHz; F2=503.2 MHz)	**26**	24.4
IP2 [dB] (F1=500.1 MHz; F2=503.2 MHz)	**64**	58.3

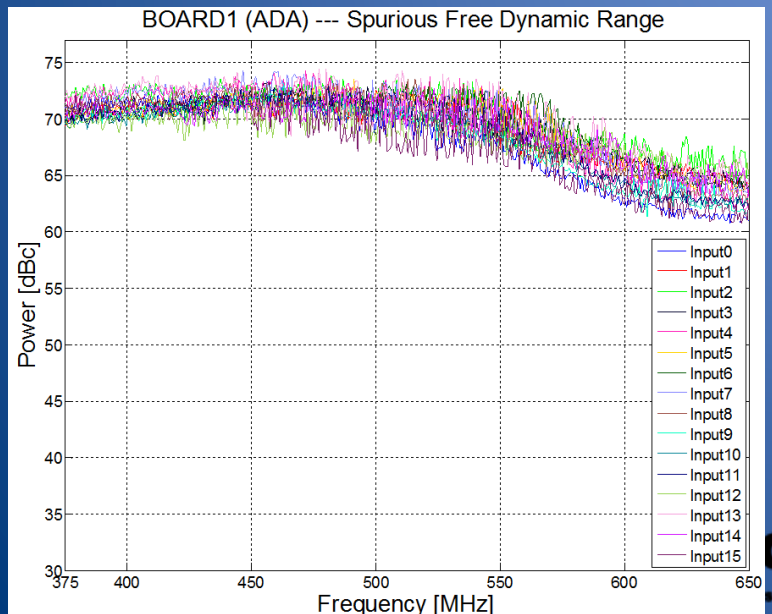
NOTE: all values are based on WORST CASE

Spurious Free Dynamic Range

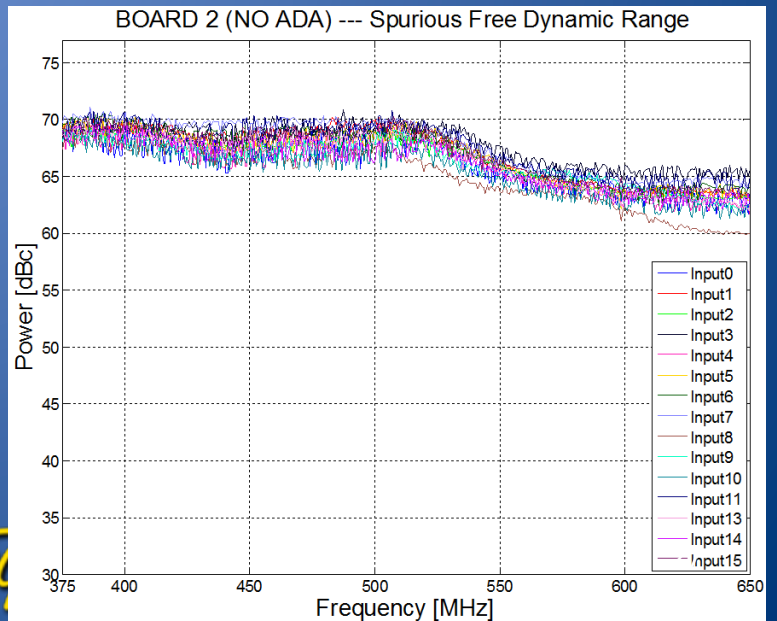


50-375 MHz

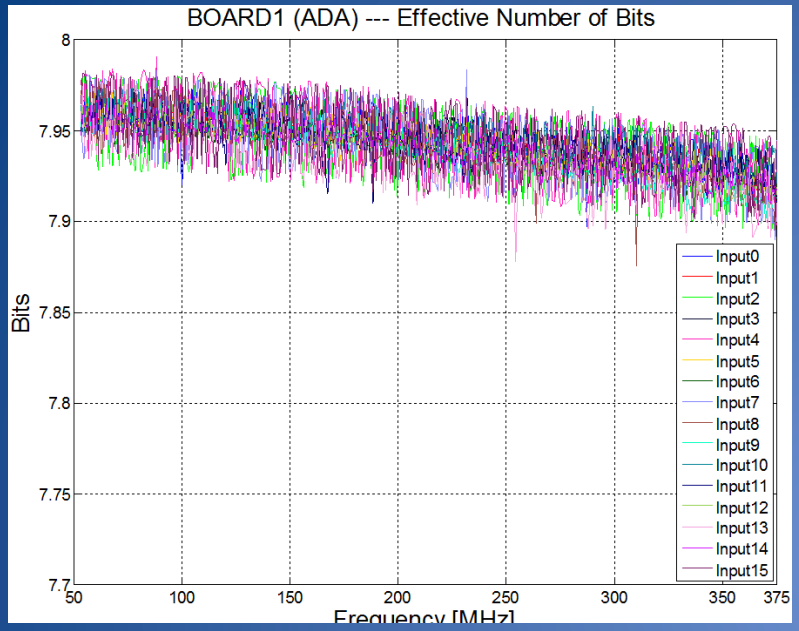




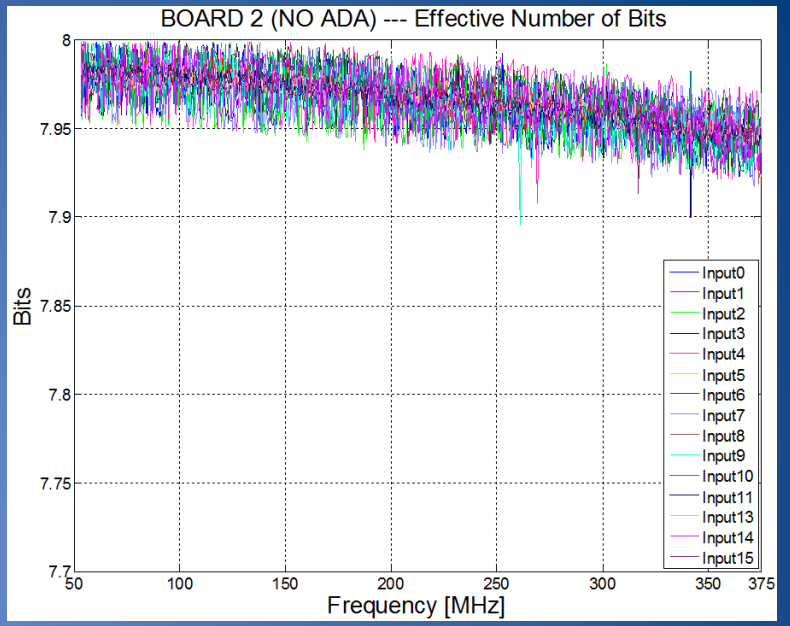
375-650 MHz

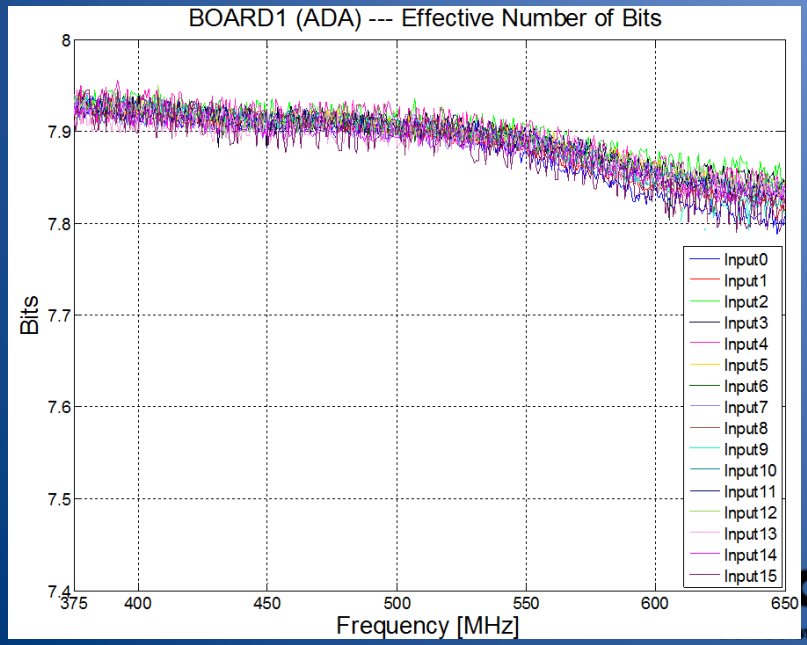


Effective Number of Bit

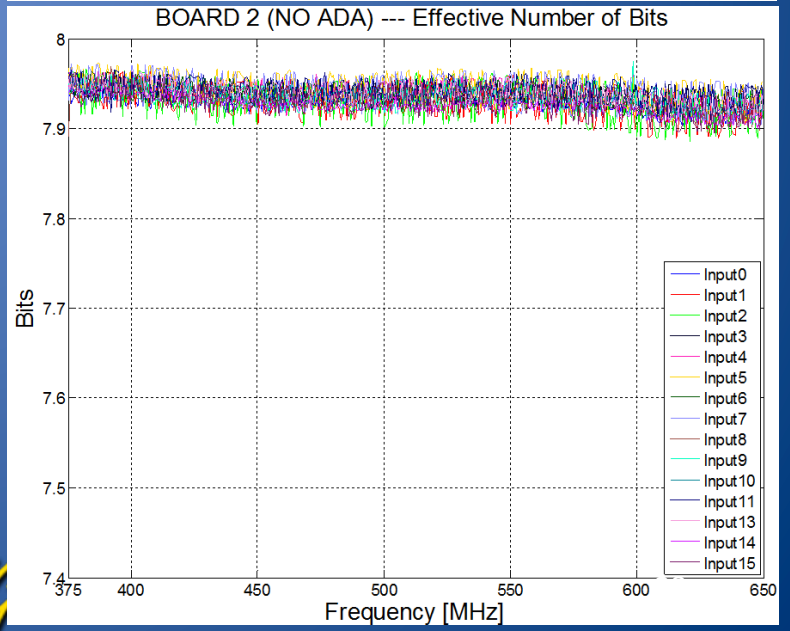


50-375 MHz





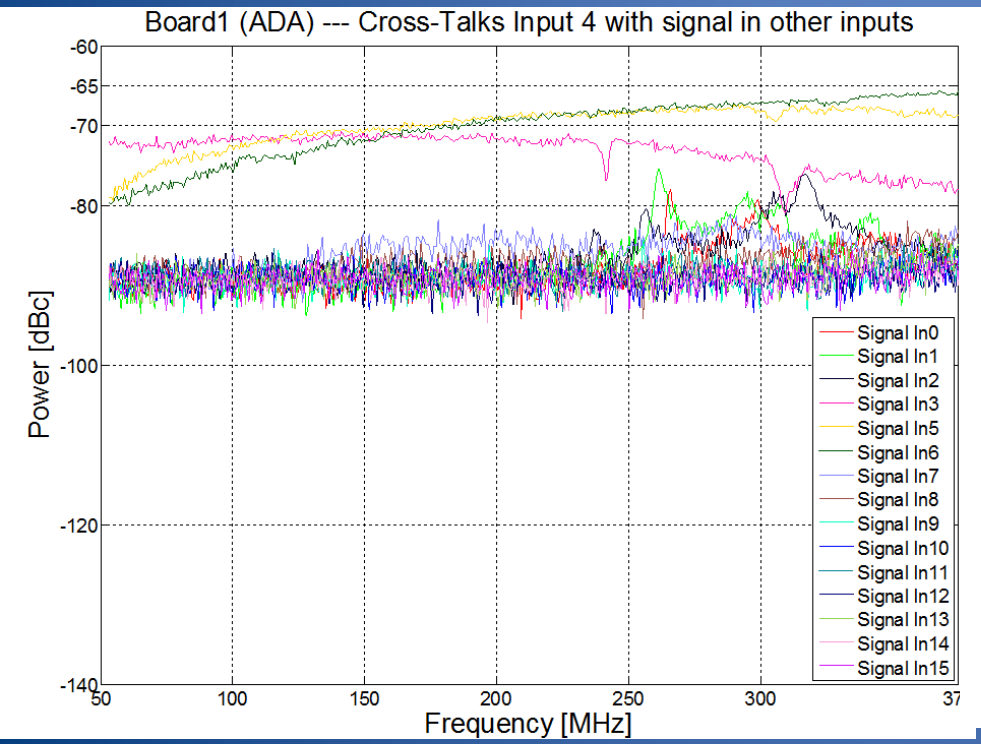
375-650 MHz

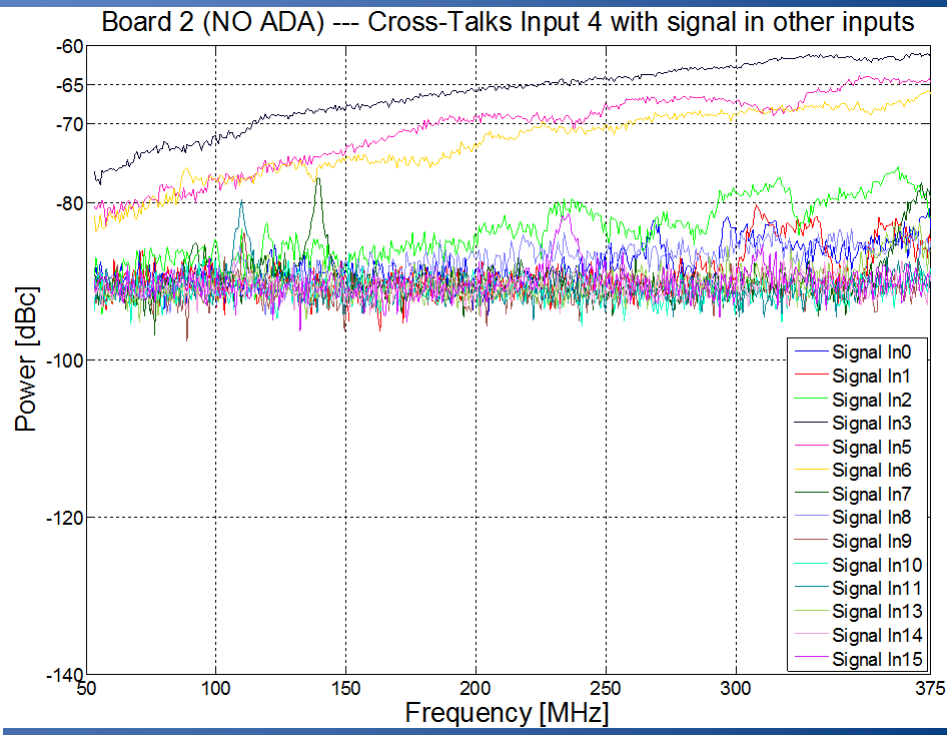


Cross-Talk Measurement

BANDWIDTH: 50-375 MHz, signal injected in Input 4, no heat sink shielding

WORST CASE





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END

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Thanks!

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