MARCO BARTOLINI - BARTOLINI@IRA.INAF.IT

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WORKSHOP: FPGA APPLICATION IN ASTROPHYSICS

FPGA APPLICATIONS FOR SINGLE DISH ACTIVITY AT MEDICINA RADIOTELESCOPES

WHO AM I ?

- Tecnologo TD @ IRA since 2012
- Computer Science
- Spent 2008 - 2011 working on FPGA technologies for radio astronomy
- At present mainly involved with SRT control software development: DISCOS

THE MEDICINA 32M DISH

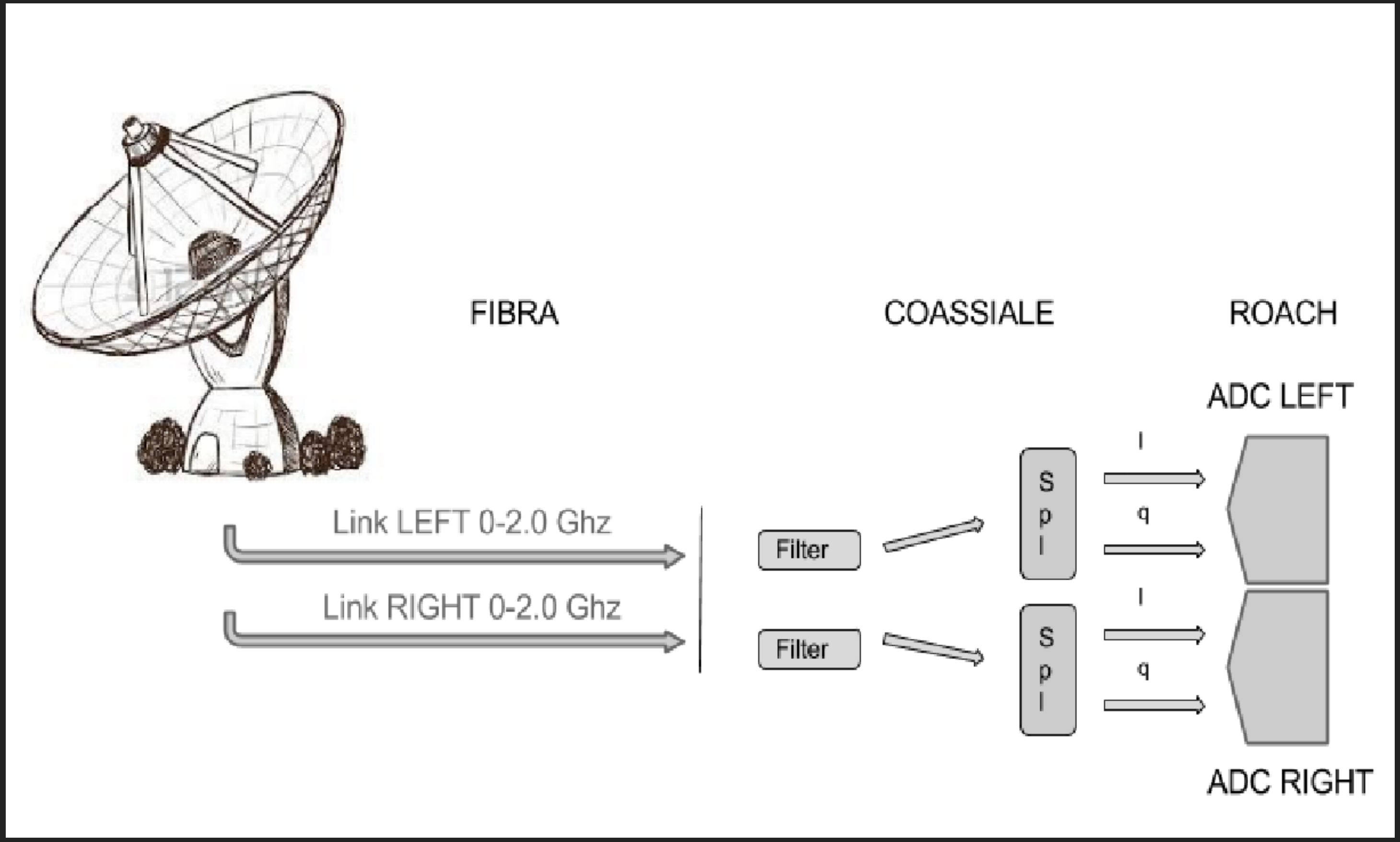
- 32m cassegrain radio telescope
- Frequency agility from 1.35GHz to 26.5GHz
- Primary and Cassegrain foci
- Completely automated observing setup
- EVN VLBI, Geodesy, Single Dish activity

I WILL TALK ABOUT

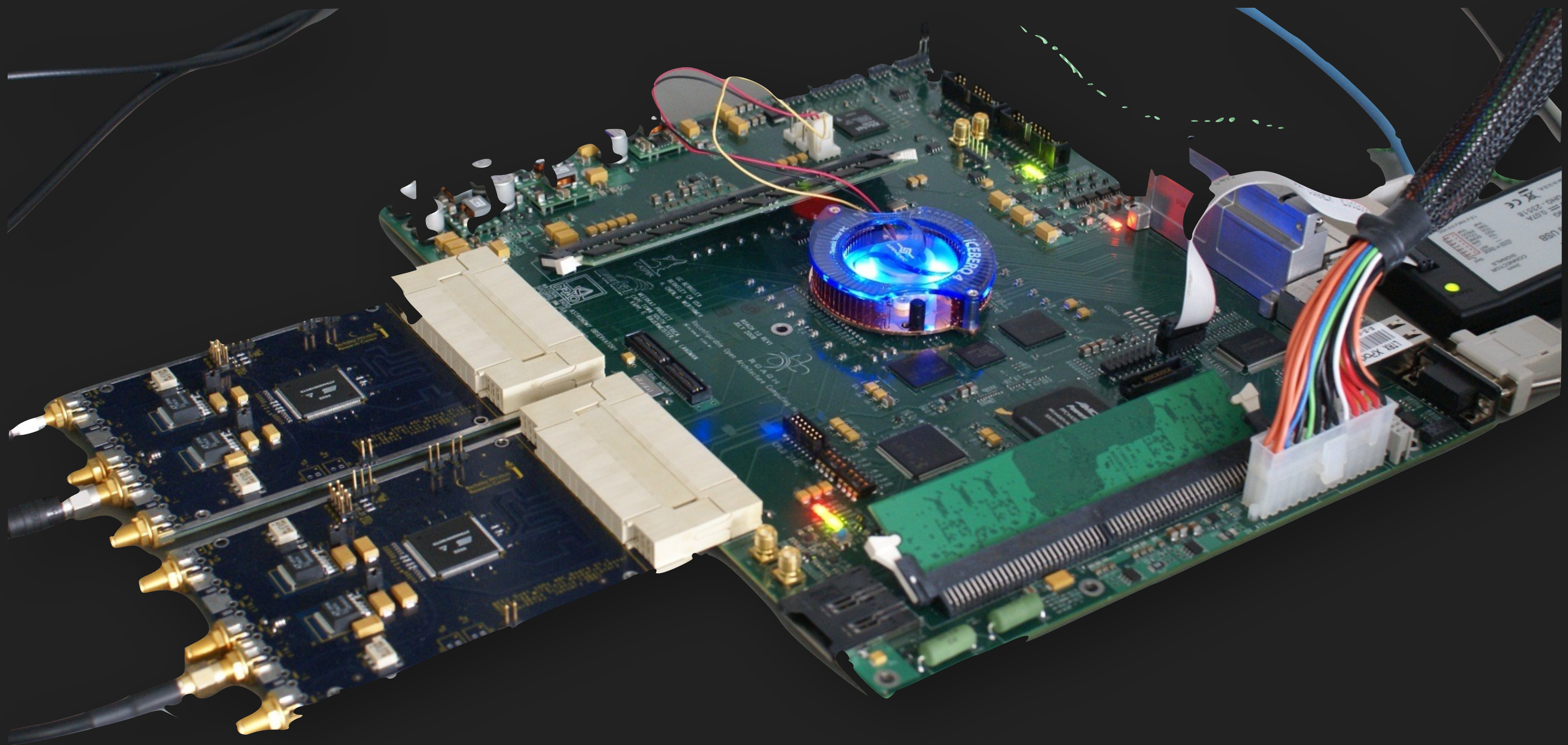
- Instrumental setup at Medicina
- Prin tecno INAF “RFI mitigation at italian radio telescopes”
- HPC Spectroscopy applications developed on ROACH boards
- FPGA boards system integration with external hardware and software
- FPGA used as control logics for custom digital backends

MEDICINA SETUP

- Every RF signal is down converted to the 0.1GHz - 2.2GHz region
- The IF signal is transmitted as RF over optical fiber to the control room
- Optical receivers convert the signal into coaxial and connect to the backends



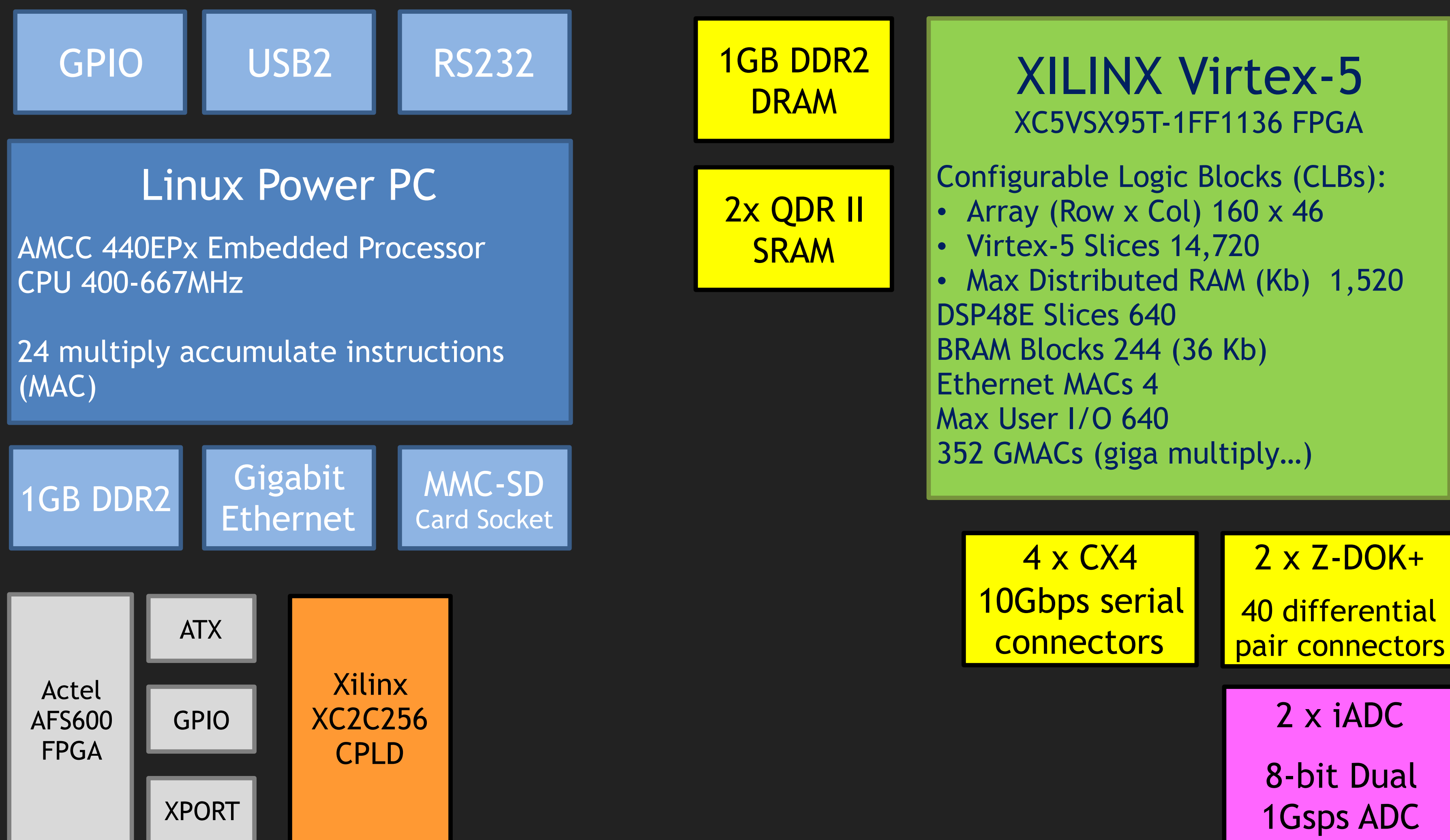
ROACH BOARD



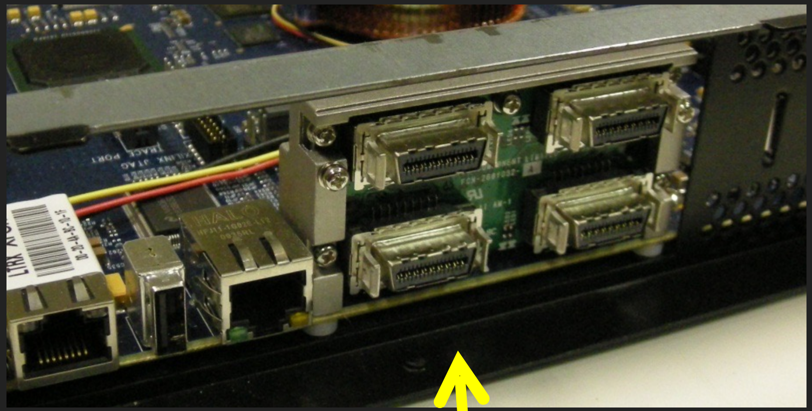
http://casper.berkely.edu/wiki/ROACH/

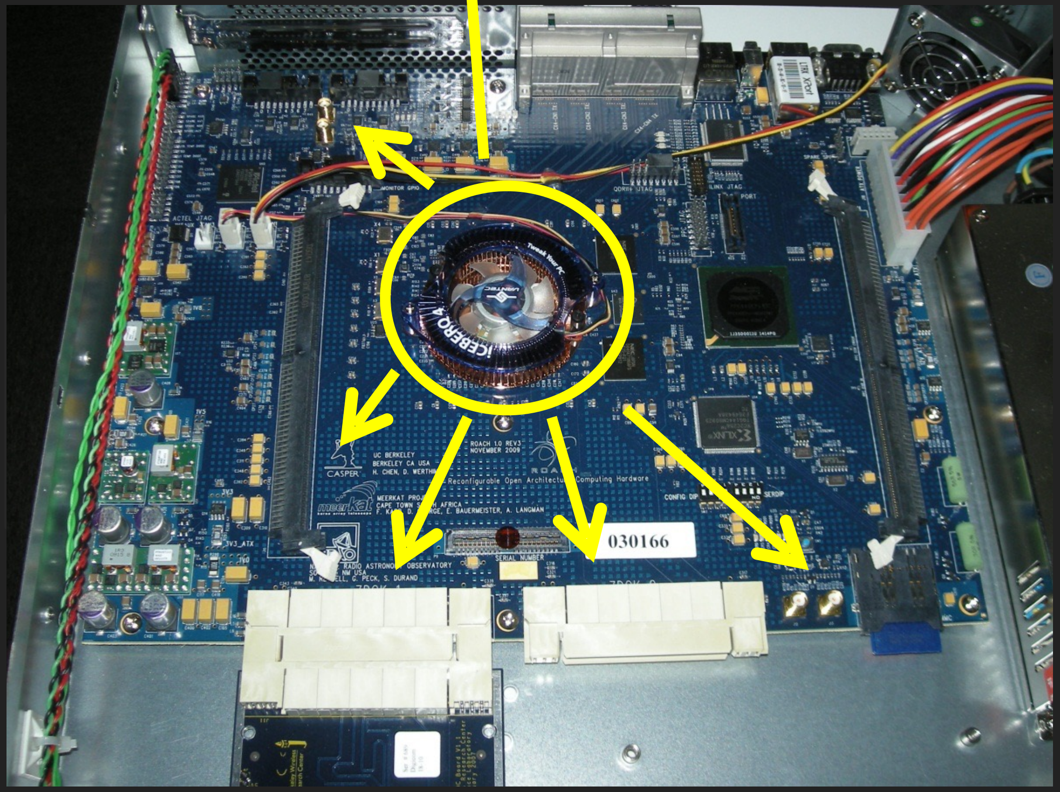
COURTESY OF ANDREA MATTANA

ROACH BOARD HARDWARE SUMMARY



ROACH BOARD I/O





1GB DDR2 DRAM

2x QDR II SRAM

XILINX Virtex-5

XC5VSX95T-1FF1136 FPGA

Configurable Logic Blocks (CLBs):

- Array (Row x Col) 160 x 46
- Virtex-5 Slices 14,720
- Max Distributed RAM (Kb) 1,520

DSP48E Slices 640
BRAM Blocks 244 (36 Kb)
Ethernet MACs 4
Max User I/O 640
352 GMACs (giga multiply…)

4 x CX4 10Gbps serial connectors

2 x Z-DOK+ 40 differential pair connectors

2 x iADC 8-bit Dual 1Gsps ADC

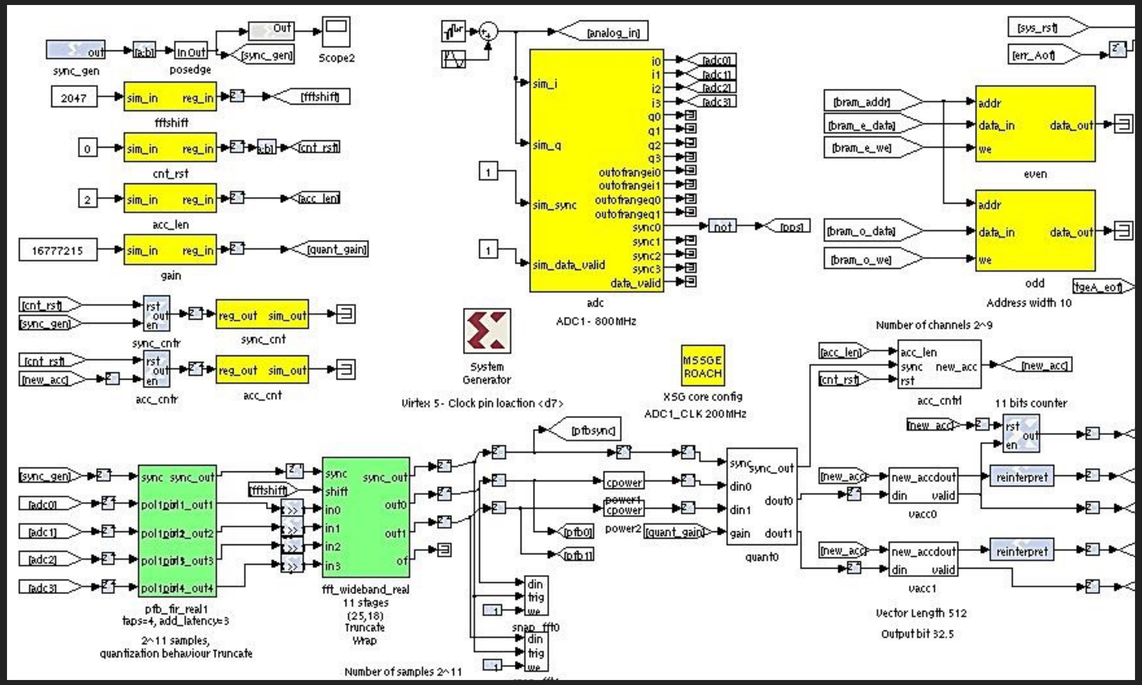
CASPER TOOL FLOW

MSSGE Toolflow

Matlab Simulink System Generator EDK

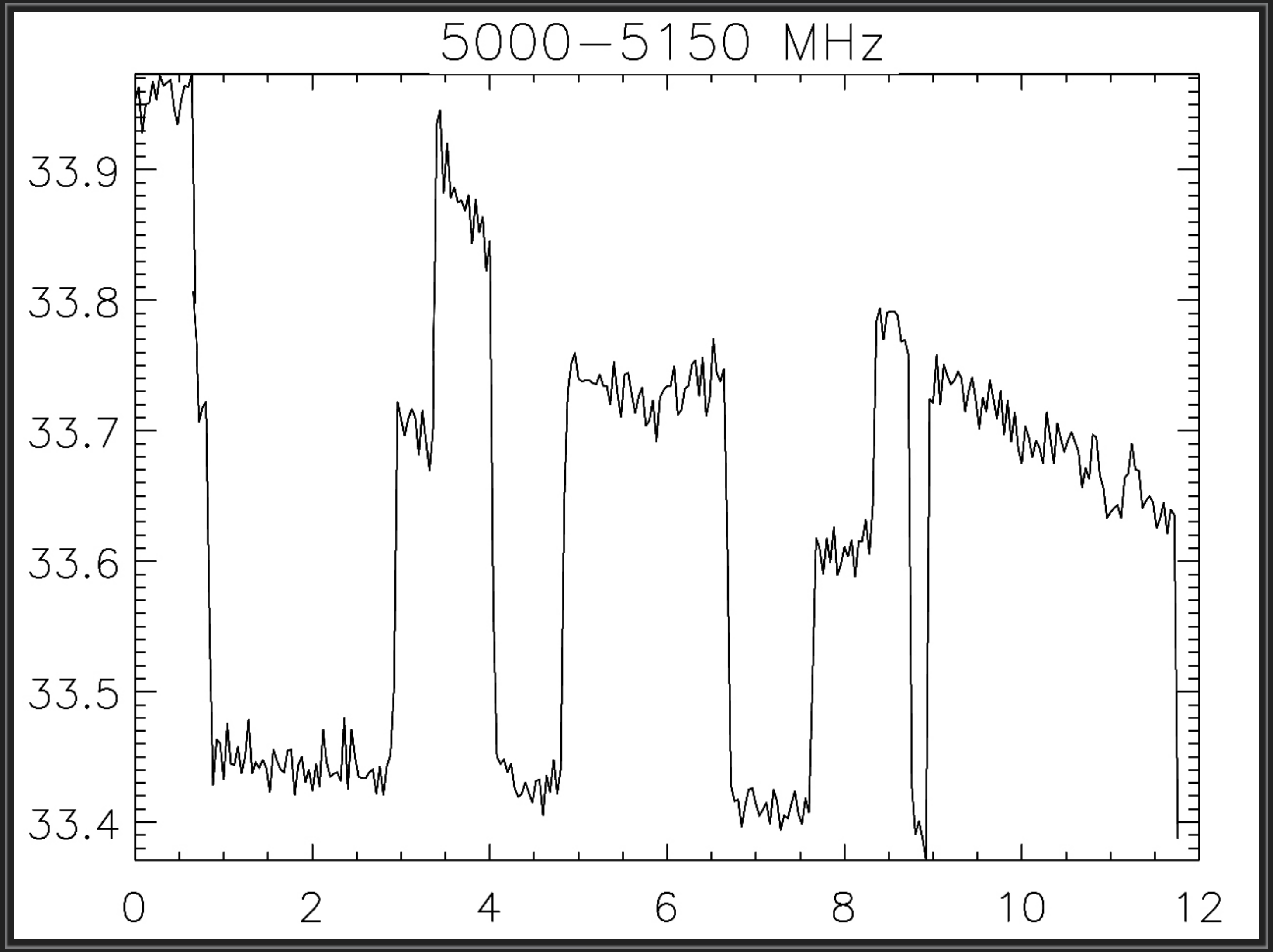
Design Flow

1. Create a Simulink model.
2. Compile with BEE XPS.
3. Program your board.
4. Test, and repeat.

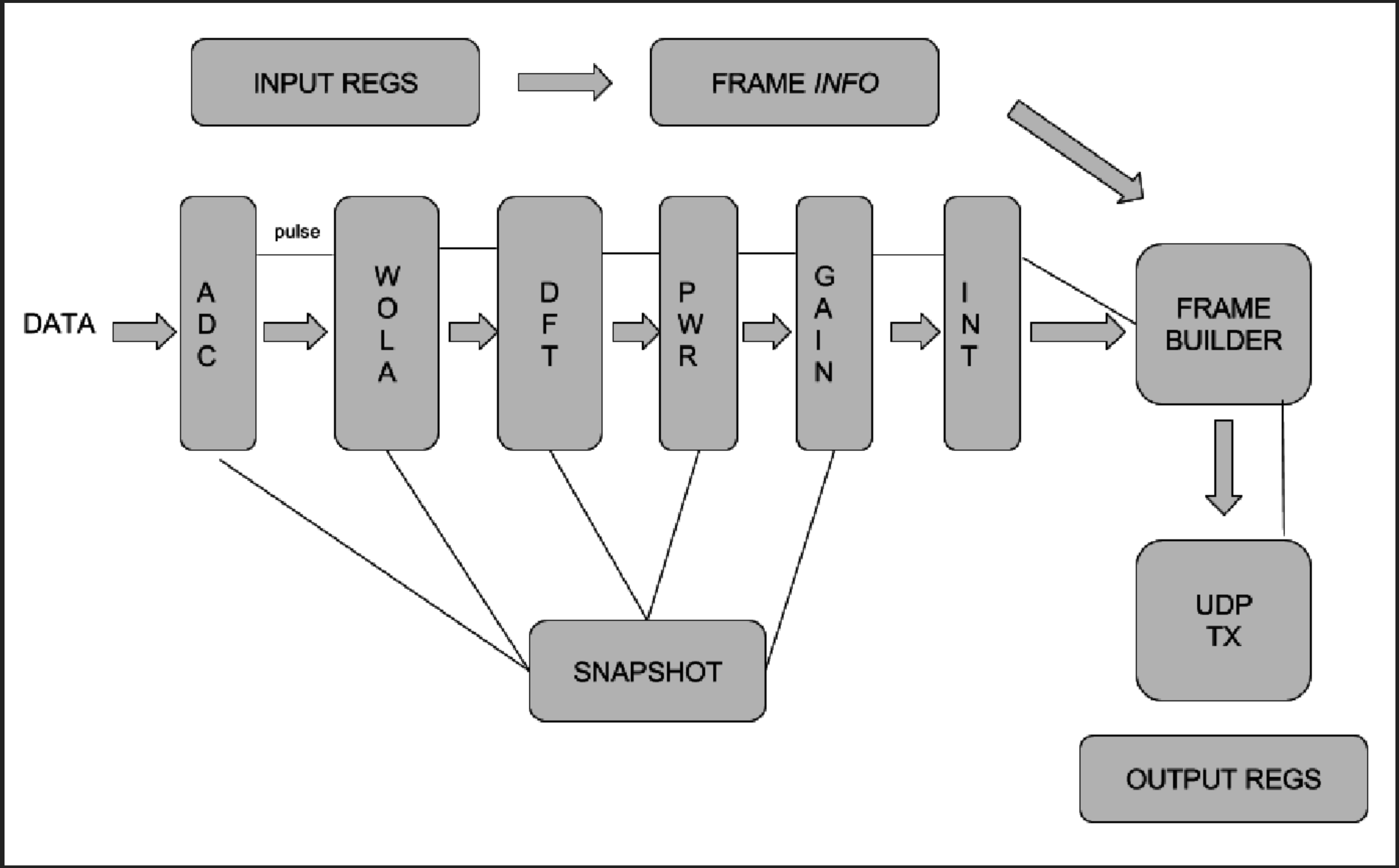


PRIN: RFI MITIGATION AT ITALIAN RADIOTELESCOPES

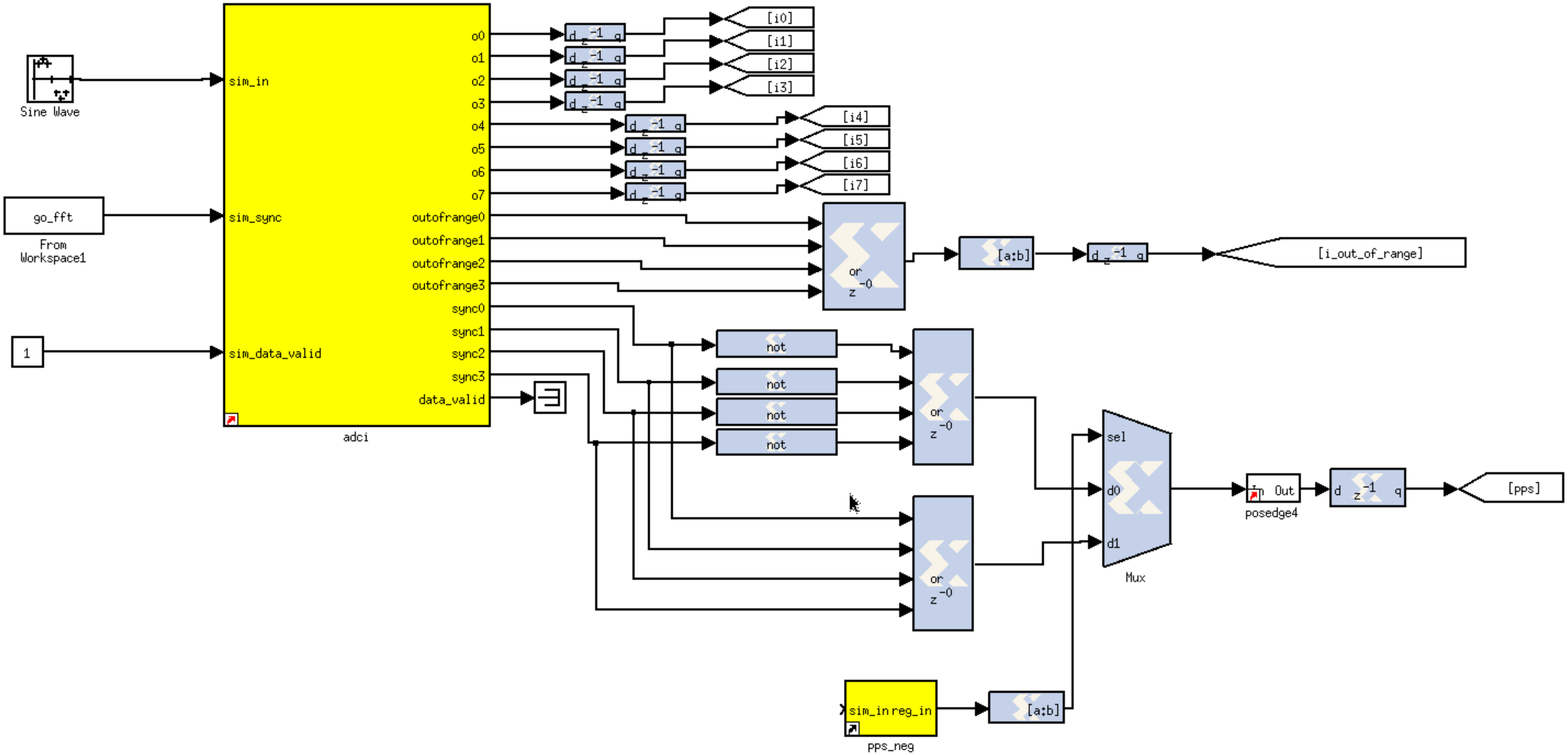
- Environment extremely polluted
- Worst cases of 70% data loss because of radio interferences
- We cannot continue to observe with large bandwidths in continuum mode
- Need to build a spectrometer



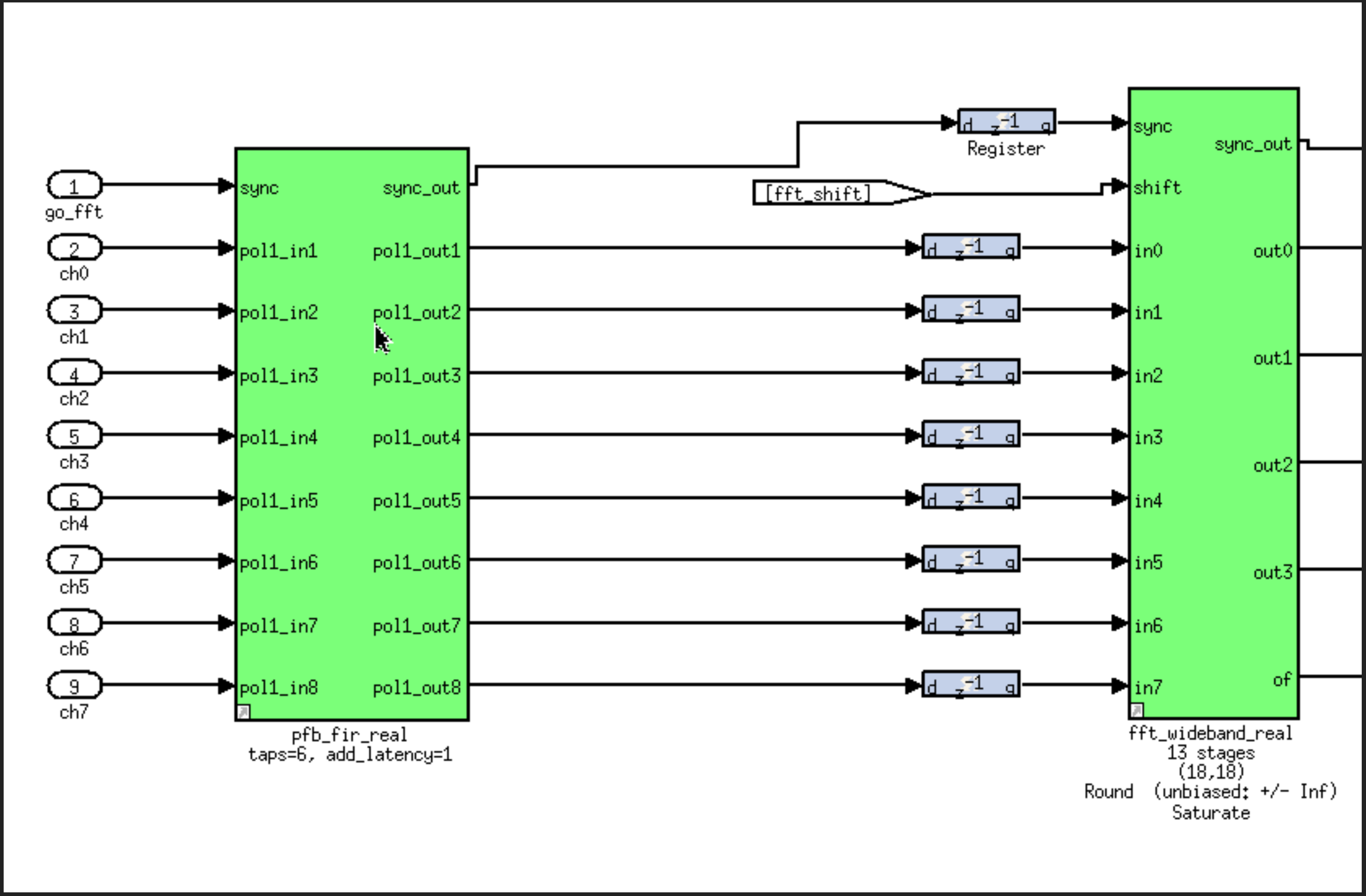
WBLGB SPECTROMETER OVERVIEW



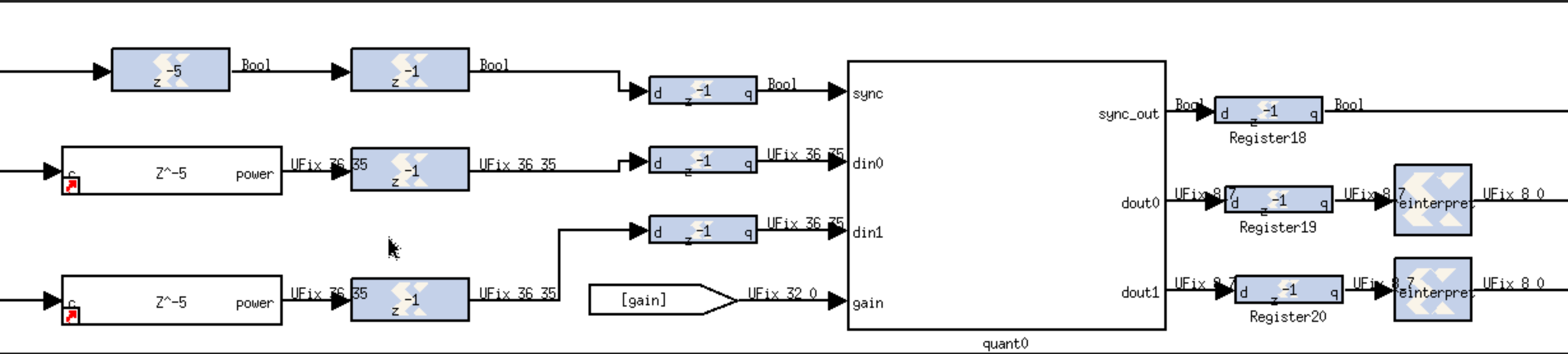
WBLGB SPECTROMETER - SAMPLING

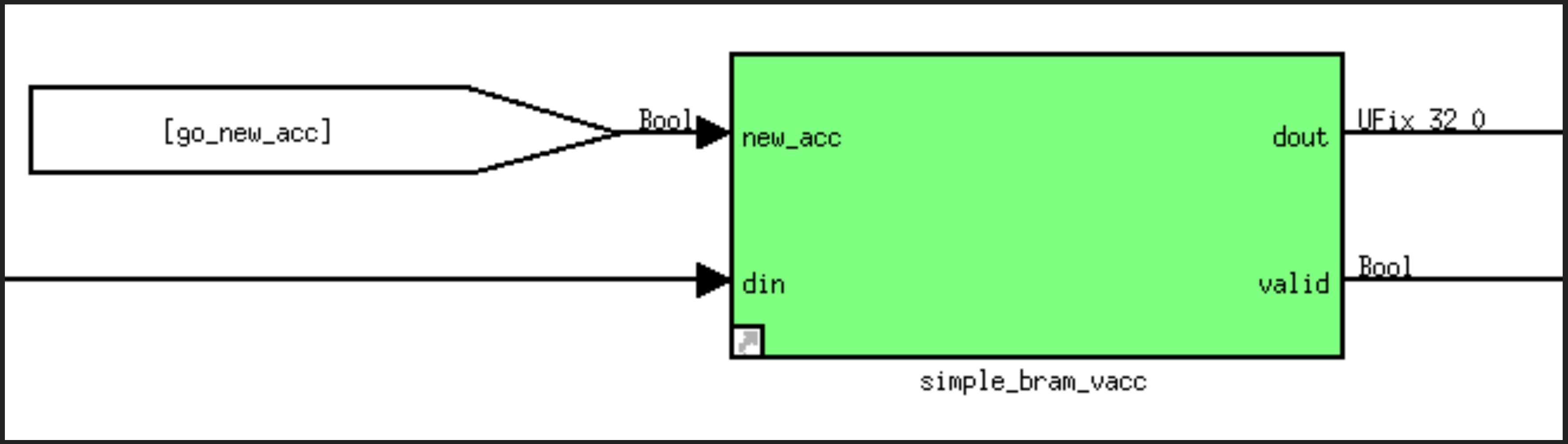


WBLGB SPECTROMETER - CHANNELIZATION



WBLGB SPECTROMETER – ACCUMULATION





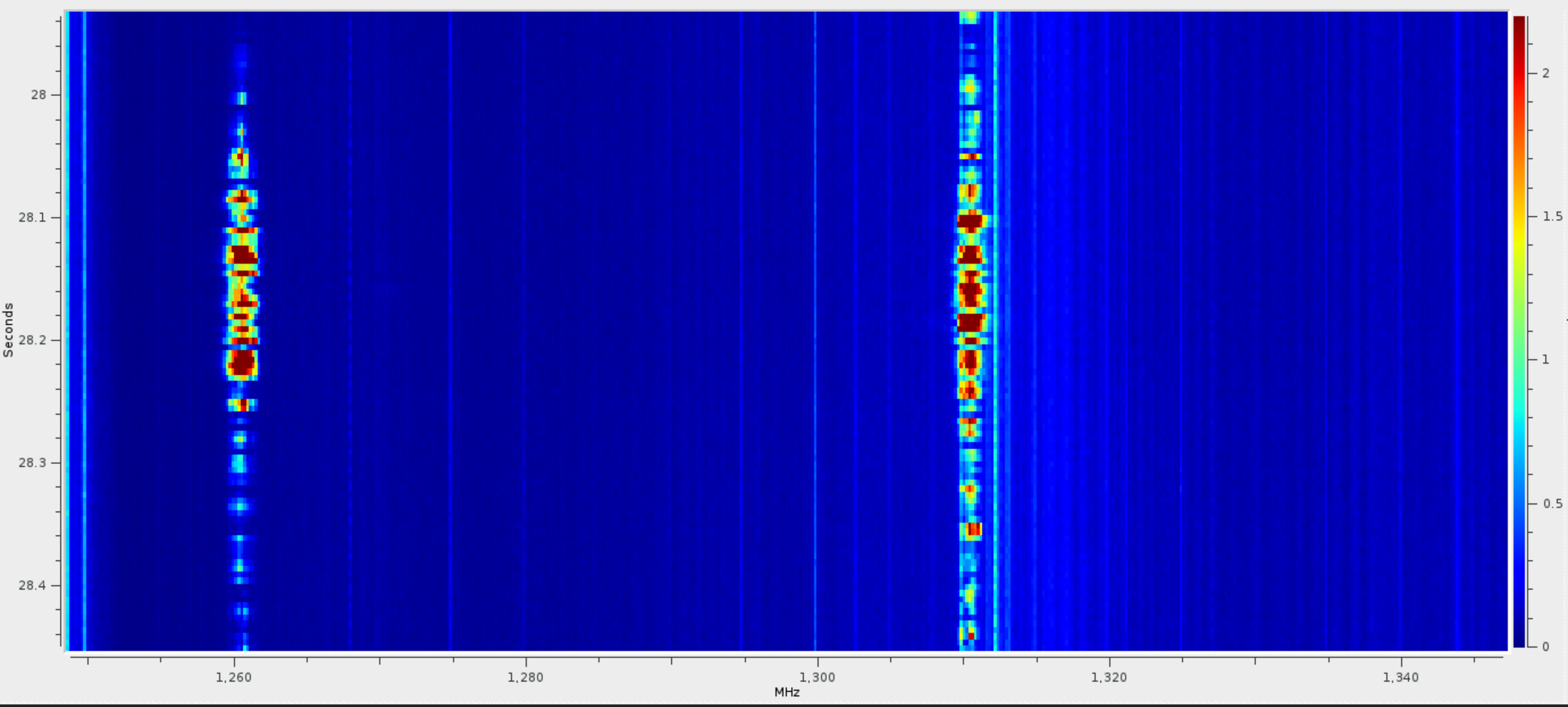
WBLGB SPECTROMETER CHARACTERISTICS

- 700MHz bandwidth
- 4096 frequency bins via PFB and FFT
- realtime data time stamping, synchronized with external clock
- configurable digital gain and FFT shift, robust to RFI signals
- overflow monitoring
- every stage inspectable via ram blocks

WBLGB SPECTROMETER PERFORMANCES

- 1ms minimum integration time for fast RFI detection
- Data input rate: 10Gbps
- Real time streaming FFT channelization
- Data output rate: 1.25Gbps

WBLGB SPECTROGRAM



DISCOS INTEGRATION

- DISCOS is the software we use for radio telescope control
- DISCOS protocol definition for external backends integration
- tcp/ip communication based on simple linefeed protocol
- available libraries from casper consortium
- http://github.com/discos/discos-backend
- http://github.com/discos

OPEN HARDWARE + OPEN SOFTWARE + STANDARD PROTOCOLS

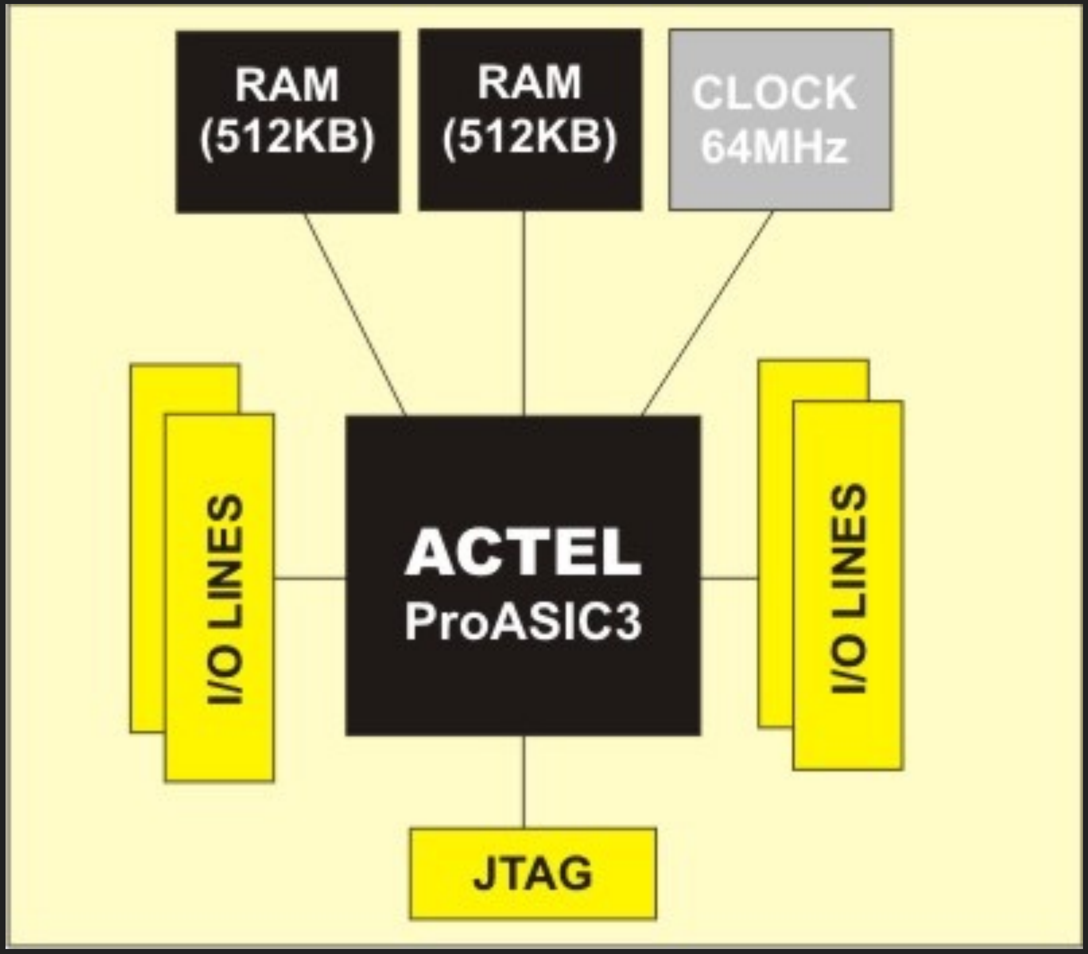
- Enable collaboration via community
- Standard infrastructures based on ETHERNET
- Shared issues -> shared solutions
- Human resources optimization
- Developed at Medicina -> deployed at Sardinia Radio Telescope (SRT)
- Developed at SRT -> deployed at MED

AN EXAMPLE: MEDARA AT MEDICINA

- Developed SARDARA at SRT
- Integrated in DISCOS control system
- Porting is planned for MEDICINA using already available hardware (ROACH2) originally thought for other projects
- FPGA technology is a key component in this workflow

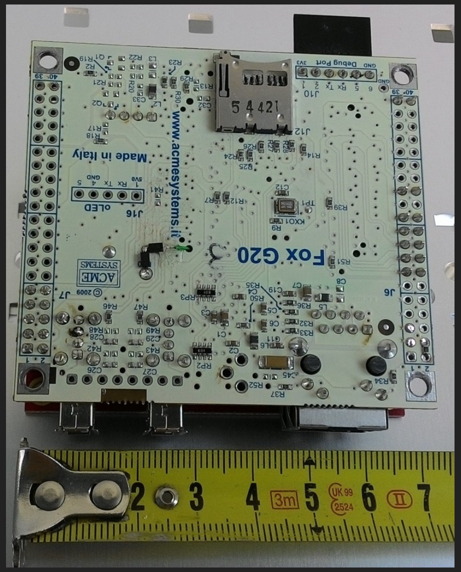
FPGAS FOR BACKEND CONTROL

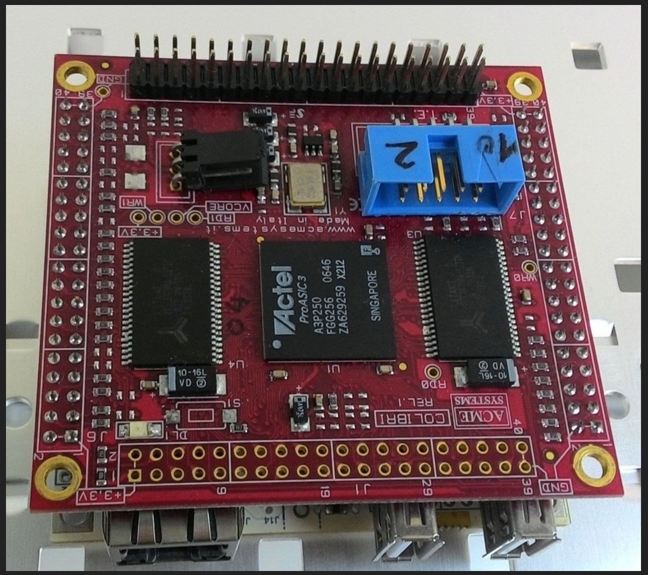
- FPGA board “colibri" from **Acme Systems** based on ACTEL A3P250
- Can be interconnected with a SBC FOX Board G20 (ARM9 @ 400MHz legacy Linux embedded board)
- The system, has been used to built the Total Power Acquisition System for SRT , Medicina and Noto radio telescope and to acquire data from Analog Pulsar Filter bank for SRT.

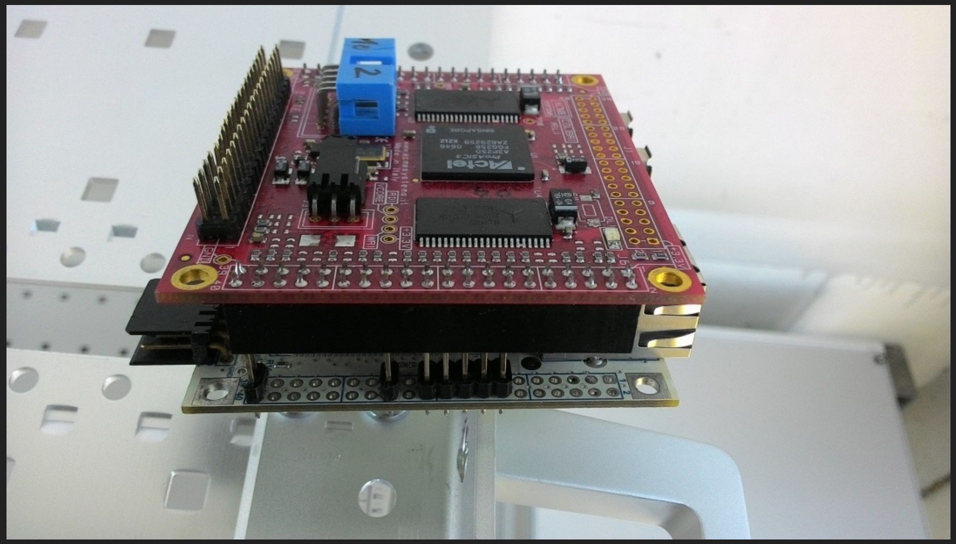


TOTAL POWER BACKEND CONTROL

- The system uses a multi channel Voltage to Frequency converter to acquire total power value. It can be interconnected with a SBC FOX Board G20 (ARM9 @ 400MHz legacy Linux embedded board)
- The FPGA is in charge of producing variable sample rate and to embed UTC epoch information into data stream.



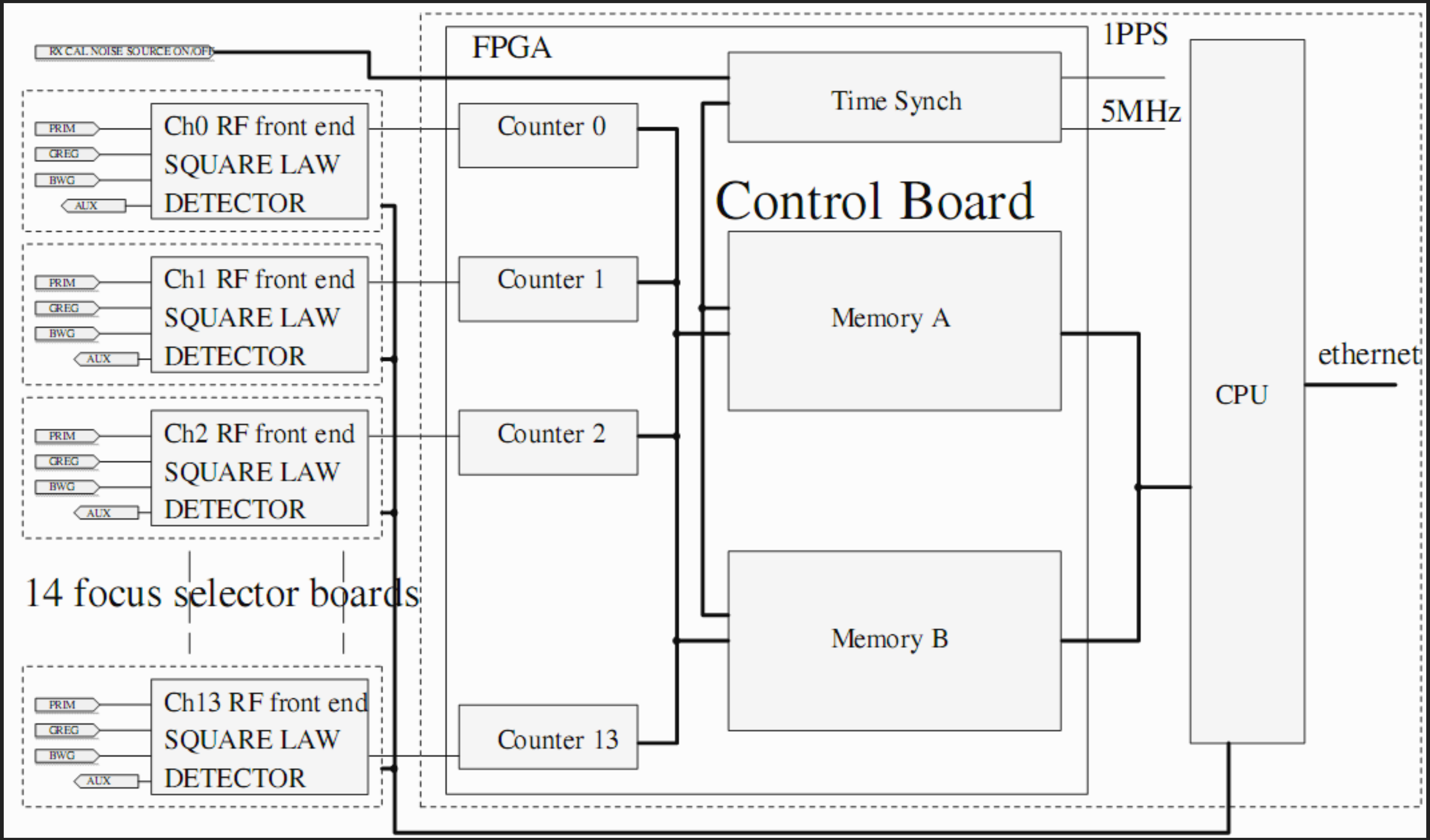




ANALOG PULSAR FILTER BANK SAMPLING

- The system consists of 1024 channel digitized at 1 bit, at each sample, all 1024 channel are stored in 16 bit words, into one memory buffer. In the meantime the CPU has access to the second memory buffer and transmits the stored samples via ethernet.
- The FPGA implement the data bus and the mux control from digitizer, the epoch counter and UTC info, the sample rate generator, the dual memory buffer management and the bus interface towards the cpu board

ANALOG PULSAR FILTER BANK SAMPLING SCHEMA



CONCLUSIONS

- FPGA used for High performance digital signal processing
- FPGA used for lower performance digital instrumentation control
- FPGA enable hardware reutilization
- FPGA enable sharing infrastructures
- High level development environments enable collaboration of non expert people, like me ;)

BUT

- Board development is a dangerous option, how long does it take? Do we release obsolete products? Do we have appropriate resources for development, production and maintenance of new products? Or can we create SPINOFFs after the research phase? Can INAF be a guide in this direction?
- FPGA are expensive
- could we access XUP via INAF or ICT ?
- Higher level formation

THE END