



FPGA IN ELETTRONICA PER MISSIONI SPAZIALI E A TERRA

Matteo M. Angarano
Sales & Marketing Manager

SITAEEL

CONFIDENTIAL SITAEEL PROPERTY

SYNERGIC HIGH-TECH COMPANIES WITH
1000+ HIGHLY SKILLED EMPLOYEES



Railway



Space



Aviation

SITAEL
● Mola di Bari, ITALY

SITAEL
● Pisa, ITALY

SITAEL
● Pisa, ITALY



SITAEL
● Forlì, ITALY

SITAEL
● Rome, ITALY

SITAEL
● Veria, GREECE





- ❑ Largest *Italian* and *privately owned* Company operating in the **Space Sector**.
- ❑ More than **300 high qualified employees** and **state of the art facilities**
- ❑ Extensive heritage in all Design, Development, Production and Qualification processes for **Small Satellites, Advanced Electric and Chemical Propulsion Systems, Earth Observation and Science Payloads, Platform and Payload Avionics** from equipment down to complex component level.
- ❑ **Leading contractors and preferred partners** for many stakeholders in several international space projects.

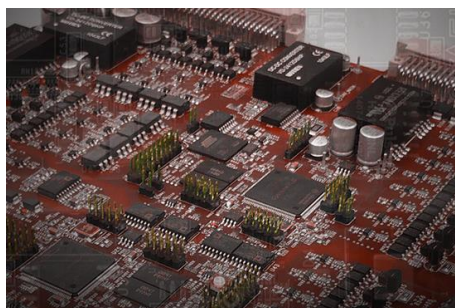
Company Profile and Business Units

The passion for high-tech and innovation led SITAEI to engage in other areas at the forefront of technology: the Industrial sector, with high-reliability electronics for **Railways** and for other safety critical applications, the emerging field of **Internet of Things** and the world of instrumentation for **Scientific** applications.



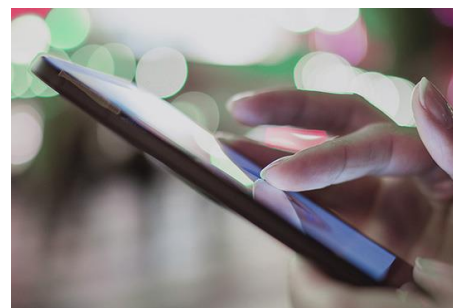
SPACE

Small Satellites, Earth Observation Services & Applications, Propulsion Systems, Instruments & Avionics from equipment down to complex component level.



INDUSTRIAL

Innovative turn-key solutions with reliable HW/SW/FW electronic applications for the implementation of tailor made services and products.



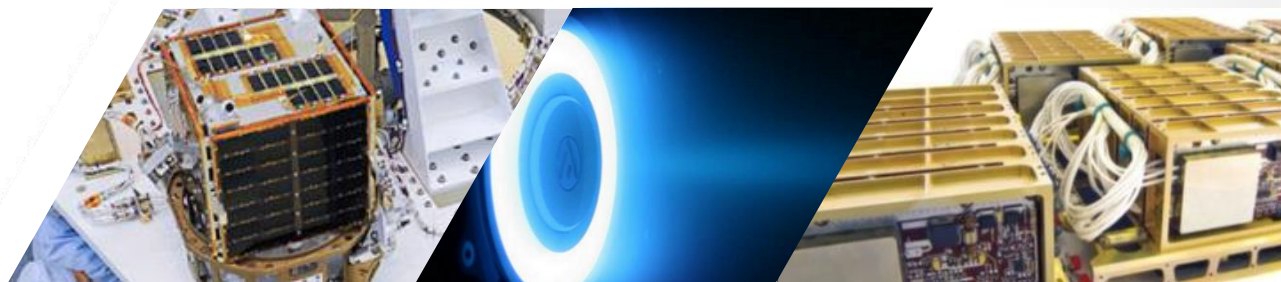
INTERNET OF THINGS

Connectivity solutions for physical objects embedded with electronics and sensors which enable remote control, data collection and exchange..



SCIENCE

Industrial partner for Big Physics; electronics design and production; sub-system assembly; applications for Environment, Safety and Homeland Security.

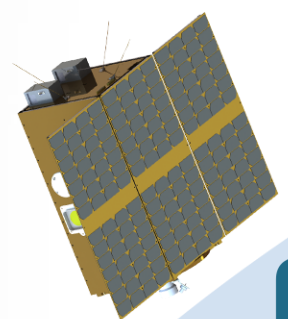


Small Satellites

Advanced Propulsion

Instruments and Avionics

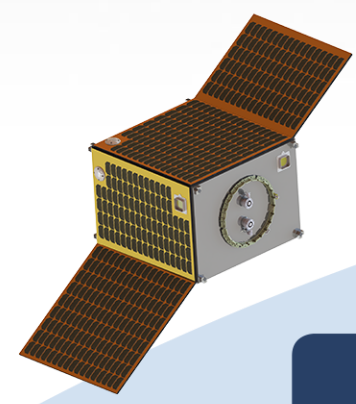
SPACE



50
kg

SITAEL S-50

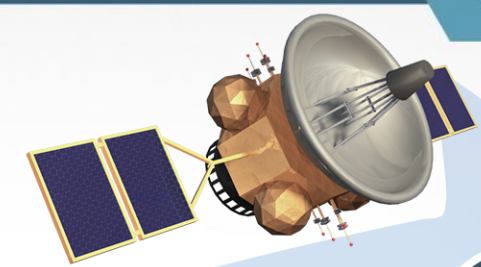
ESEO S/C (ESA)
Launch End 2015



75
kg

SITAEL S-75

- Low cost missions
- IOV/IOD applications
- EO (Low Res. image looking)
- Small EO constellation (TIR)
- For P/L up to 20kg / 30W



200
kg

SITAEL S-200

- Wide range of EO missions
- Multi-purpose platform
- EO missions:
 - High Res. PAN-VIS
 - NIR/SWIR/TIR
 - Multi-spectral P/L
- Small EO/TLC constellation
- For P/L up to 80kg / 120W

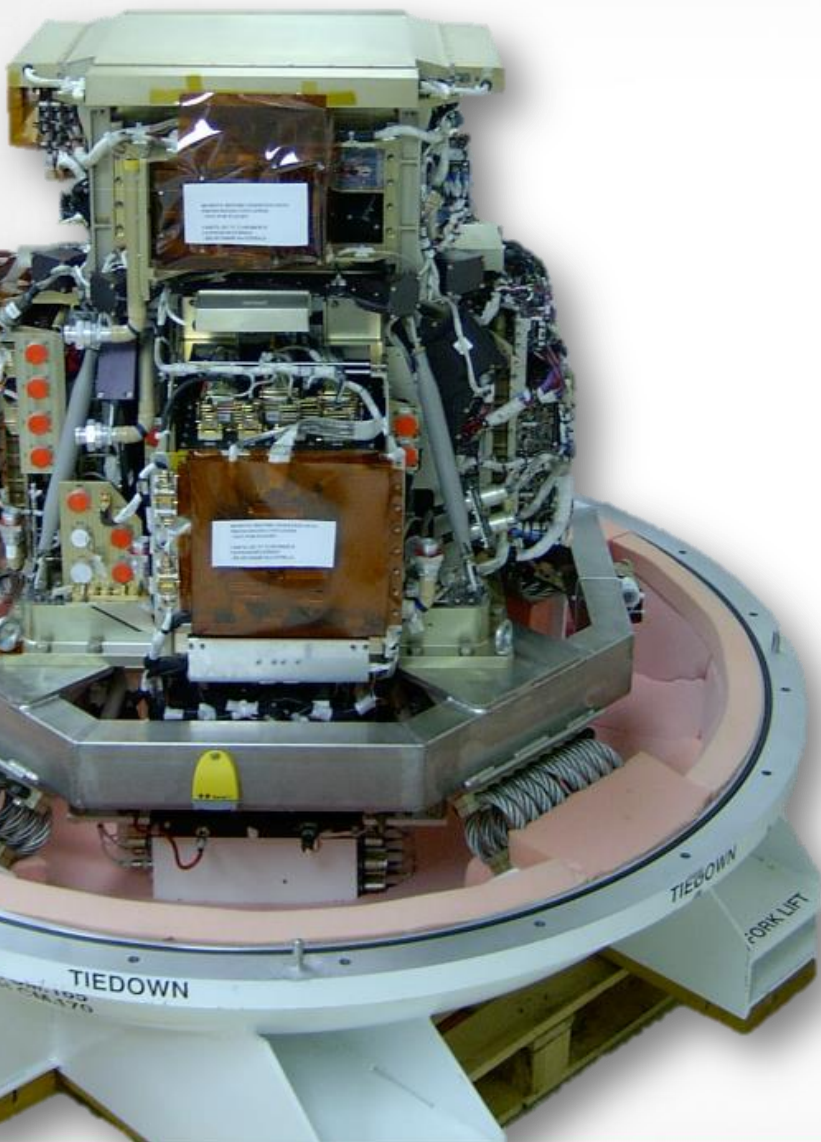
300
kg

SITAEL S-300

- More demanding missions
- EO missions:
 - High Res. Hyper-spectral
 - Small SAR missions (bistatic)
- Small Telecom missions (HTS constellations in LEO and MEO)
- For P/L up to 100kg / 1kW



INSTRUMENTS AND AVIONICS



- Detector selection and assembly
- Power, Front-end, Read-out, DAQ and Control Electronics Design, Production, Test and Verification
- Microelectronics (ASIC/FPGA) Design, Test and Verification
- Mechanical Design
- Cooling sub-system selection
- Instrument Integration
- Commissioning and Maintenance



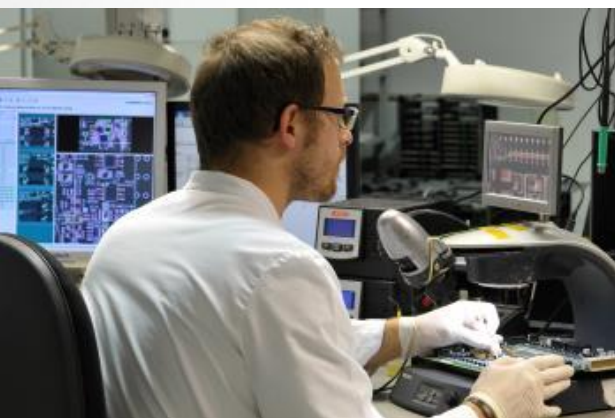
□ Design

- Feasibility study/product specification
- FW/SW development
- Design Analysis (FMECA, PSA, Radiation, ...)
- Schematics, Layout, Mechanical design
- Prototyping
- Rad-tolerant ASIC/FPGA Design & Layout



□ Production

- Space qualified manual assembly in SMT and THT
- High-Rel Automatic Assembly in SMT and THT
- Coating, Potting, Anodization
- Automatic Optical Inspection (AOI) and X-Ray (XCT) ctrl
- System integration
- ASIC manufacturing and assembly management



□ Test

- Functional and Electrical Characterization
- Environmental (TVT, Vibration, Shock), EMC
- Radiation Verification Test Management
- ASIC Screening and Qualification Management
- FPGA PPBI Management



❑ Power

- High Voltage, Low and Medium Voltage
- Applications: Optical and RF Payloads, CDMU, PCDU

❑ Control

- Complex control loop
- Applications: Propulsion, Mechanisms, Power, Cryogenics

❑ Data Handling/Processing

- Single Board Computers
- Satellite Management and Instrument Control

❑ TM/TC

- SDR technics
- UHF/VHF/S/X-Band

❑ Memory Modules

- NAND-flash based
- Radiation Mitigation

❑ Proximity Electronics

- PreAmp
- Analog Front-End
- A/D & D/A Conversion

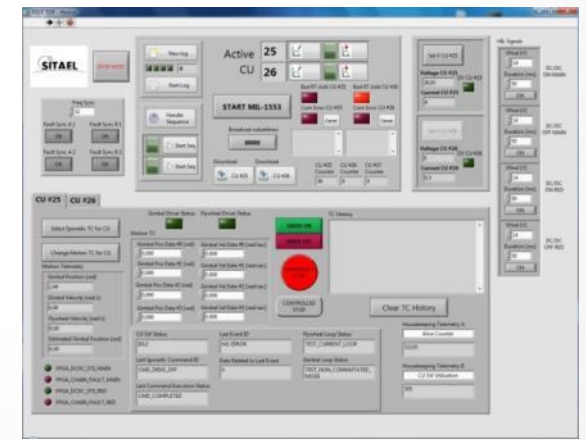
❑ CDM Development System

- LEON2-FT Processor Dev Module
- FPGA Dev Module
- CANopen Dev Module
- Memory Dev Module
- TM/TC Dev Module
- AOCS Dev Module



❑ Flight Unit Testers

- Power/Control/Data
- Custom Modules
- Hardware Racks
- Application Software



METIS Power Processing Unit

- Cold redundant architecture
- CPU module with Microsemi RTAX2000 FPGA
 - co-processing, compression, on-board algorithms
- VLDA module with RTAX1000
 - Pre-processing, filtering
- UVDA module with RTAX1000
 - Pre-processing, filtering
 - Photon counting (provided by INAF)
- Power Supply Modules



SWA Data Processing Unit

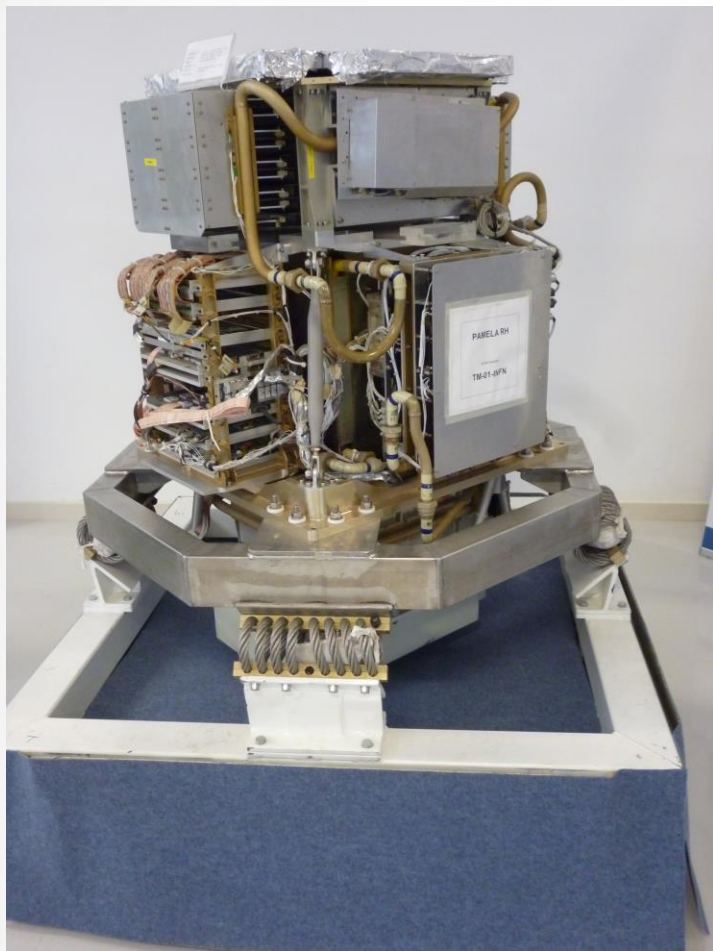
- CPU module with LEON2-FT ASIC
 - Communication with companion FPGA board
- Power Conditioning and Distribution Module





Utilizzata FPGA commerciale ACTEL (Microsemi) A54SX32A-TQ144I con circuitistica interna per la protezione al SEU ed esterna per la protezione al SEL

- DAC CONTROLLER: FPGA che genera 40 segnali a modulazione di durata (PWM) utilizzati per il controllo di DC-DC converter



Utilizzate 9 FPGA commerciali ACTEL (Microsemi) A54SX32A-TQ144I con circuitistica interna per la protezione al SEU ed esterna per la protezione al SEL

- RAM CONTROLLER: FPGA per il controllo della memoria RAM presente sulla scheda di acquisizione
- FLASH CONTROLLER: FPGA per il controllo della memoria FLASH presente sulla scheda di acquisizione
- DSP CONTROLLER: FPGA per il controllo del DSP (DSP2187L) presente sulla scheda di acquisizione
- TOF CONTROLLER: FPGA per il controllo dell'elettronica di front-end e del controllore DSP presente sulla scheda per la misura del Time-of-Flight.
- TRIGGER CONTROLLER: FPGA per il controllo del digital signal processor (DSP2187L) presente nella scheda che genera il Trigger.
- COUNTER CONTROLLER: 4 FPGA per il controllo dei contatori di: alive/dead-time, rate meters, dei segnali di piano del TOF e della rate di trigger della scheda di trigger.





Solar Orbiter METIS (*OHB, ASI, ESA*)

Power and Processing Unit for the METIS Coronagraph.

Solar Orbiter SWA (*ASI, ESA*)

Data Processing Unit for the Solar Wind Analyzer

Solar Orbiter STIX (*ESA*)

High Voltage DC/DC Converter for Spectrometer/Telescope for Imaging X-rays



JUICE (*TAS, ASI, ESA*)

RIME DES Power Generation Module & SpaceWire Test Equipment



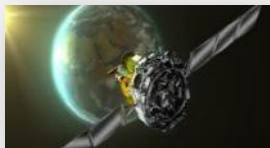
ASIM (*TERMA, ESA*)

HV Power Supply System for Atmosphere-Space Interactions Monitor (ASIM) to be installed on ISS Columbus Module



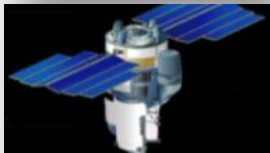
Orion MPCV (*Selex ES, Airbus DS, NASA*)

120V/28V DC/DC Converter Module of the Service Module PCDU of NASA Multi Purpose Crew Vehicle



INTEGRAL (*IAS, ESA*)

HV Power supply systems for Microstrip Gas Chambers



PAMELA (*ASI, INFN, CNR*)

Sensors and Electronics Integration for all Instruments



AMS-01/AMS-02 (*NASA, ASI, MIT, INFN*)

Sensors and Electronics Integration for all Instruments



CALET (*JAXA, NASA, ASI*)

HVPS for APD and PM sensors of CALET Experiment on ISS Japanese Module

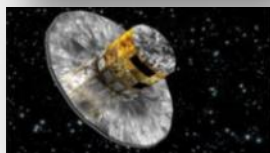
ATV (*RSC-Energia*)

CASA-2 CANbus 2.0 Controller ASIC



MSL/CURIOSITY (*NASA, Airbus DS*)

Rover Environmental Monitoring System ASIC



GAIA (*Syderal, ESA*)

Power Supply Boards for Payload Data Handling Unit (PDHU)



ASTRO-H (*JAXA, ESA*)

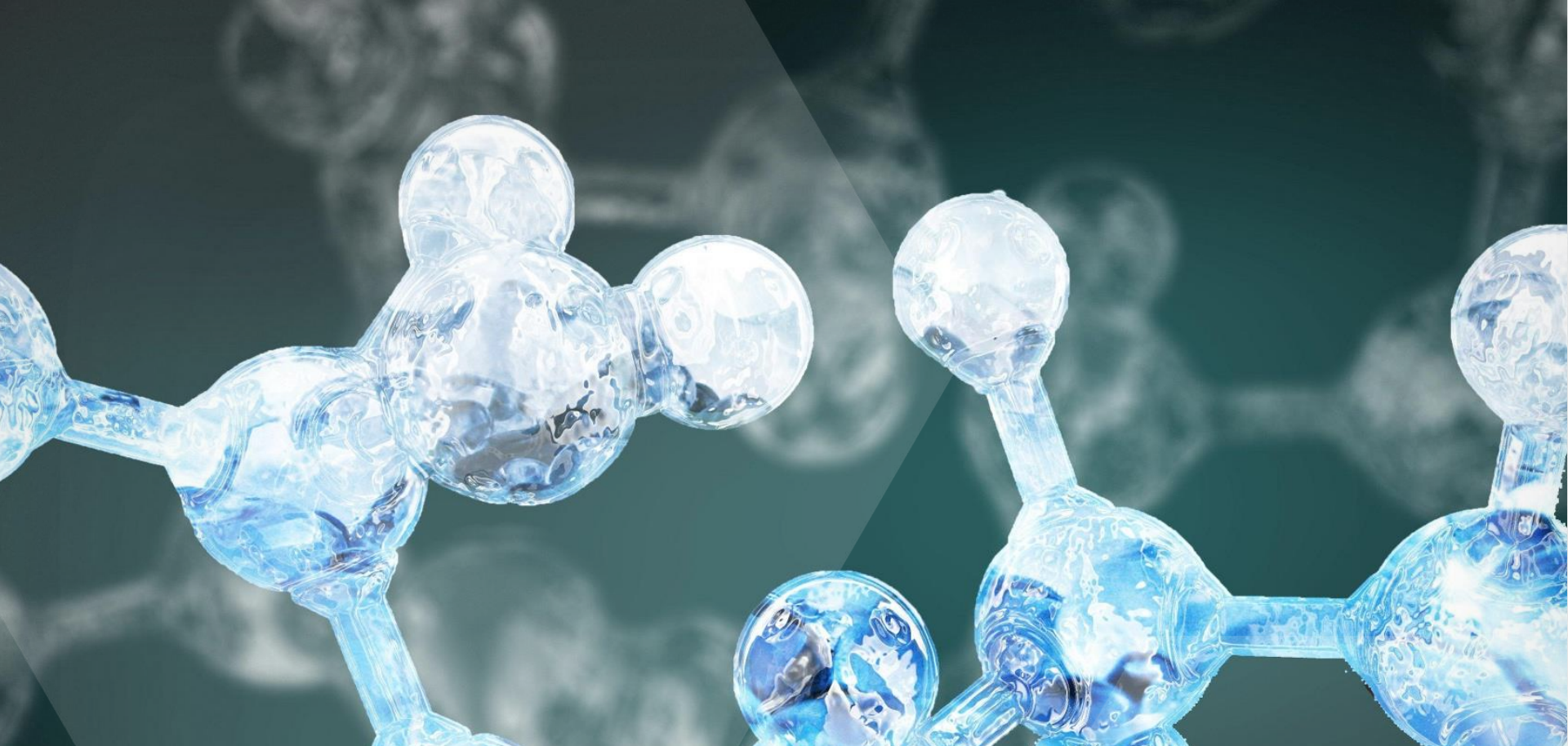
HV Power Supply systems for APD, CdTe and PM sensors



EXOMARS (*Thales Alenia Space, ESA*)

CANopen Controller IP Core





SCIENCE

SITAEEL

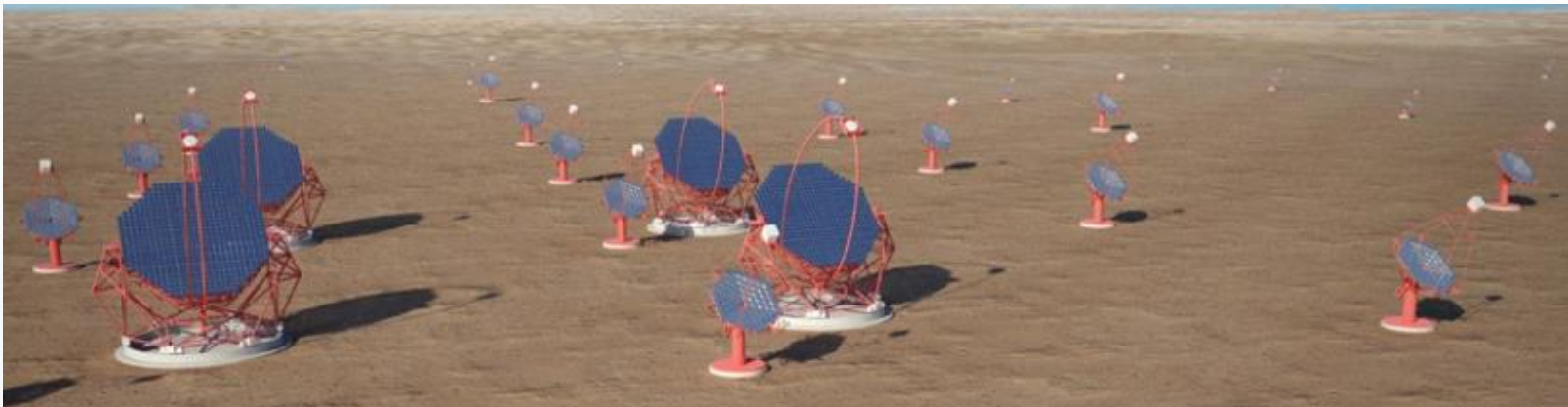
CONFIDENTIAL SITAEEL PROPERTY

Big Physics

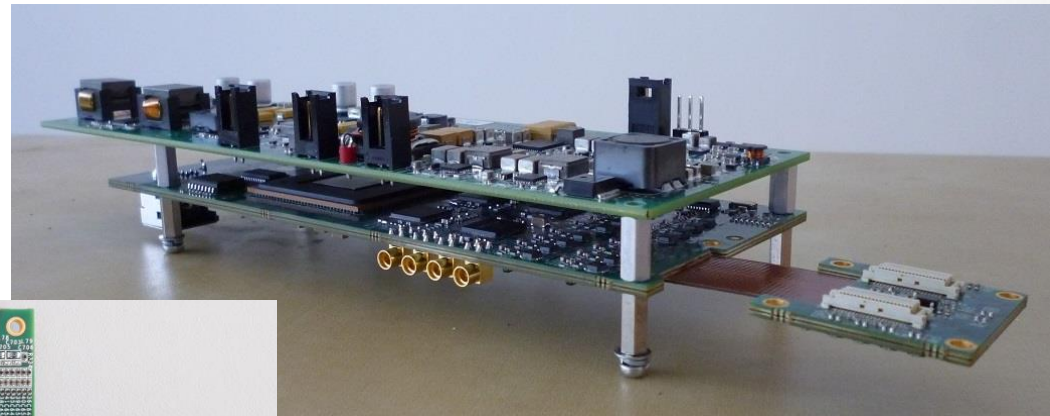
Industrial partner of Research Institutes and Universities for Big Physics projects.
On-going collaborations with Universities and INFN to develop a SiPM-based camera for CTA
(Cherenkov Telescope Array)

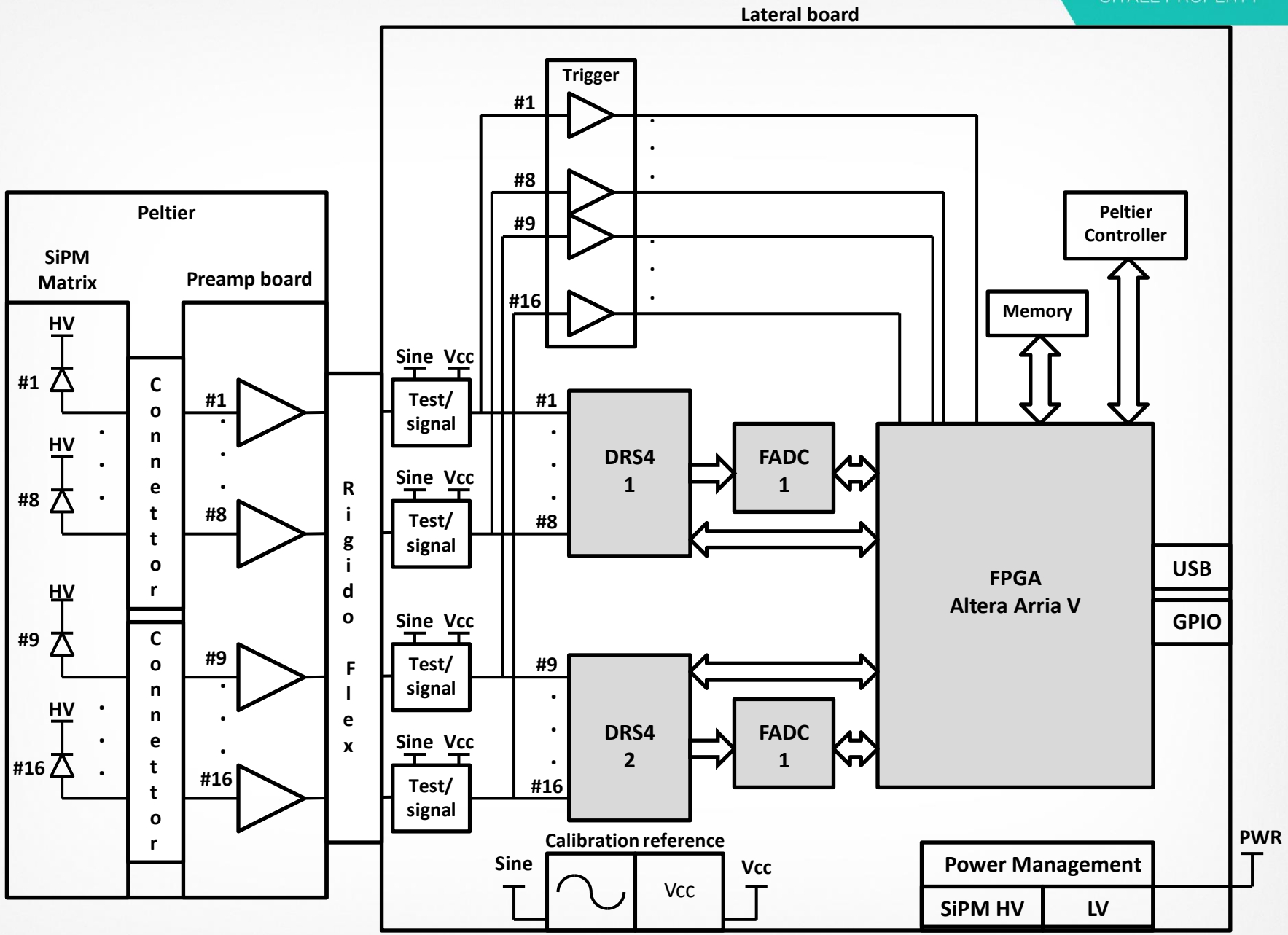
Capabilities

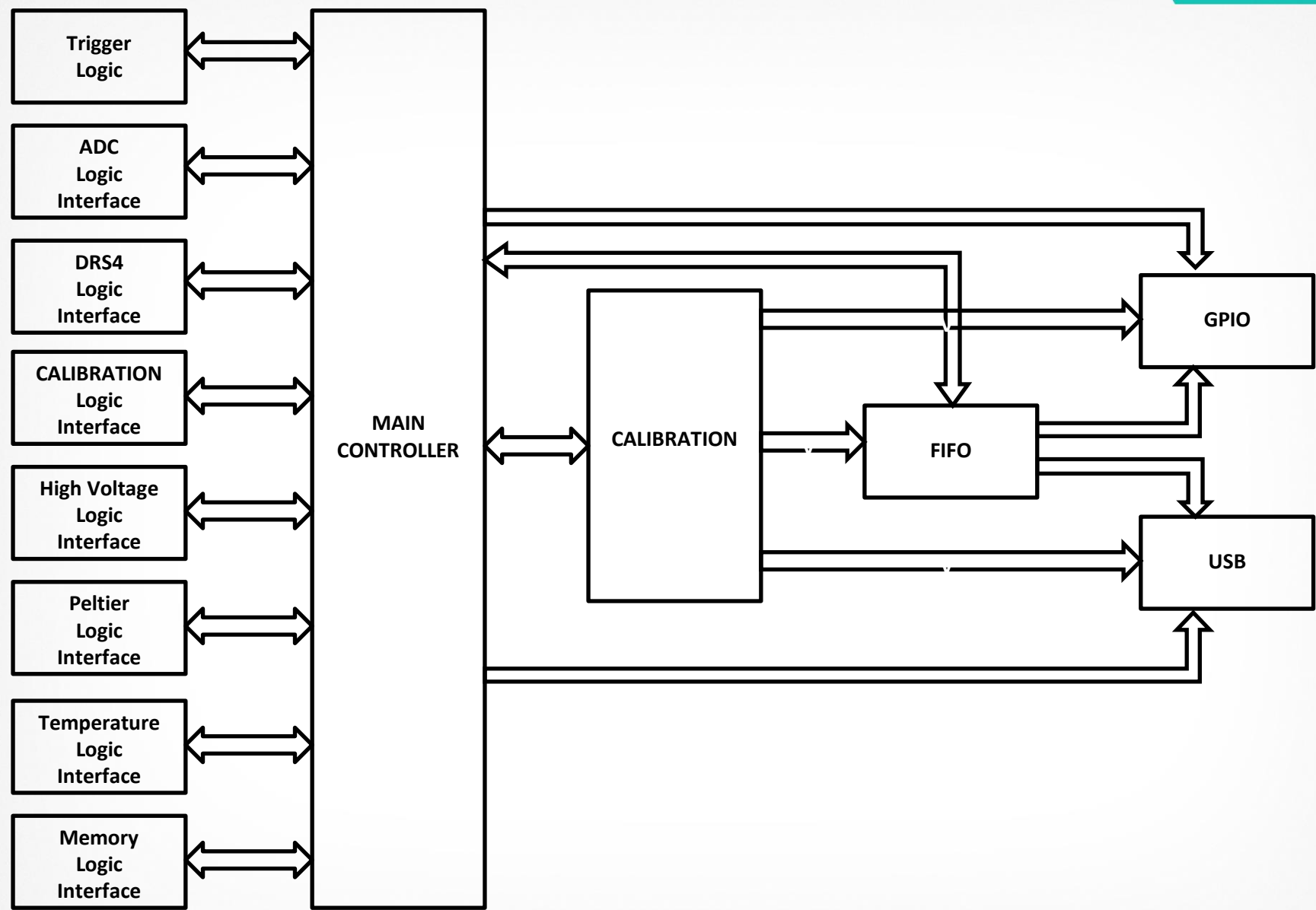
- Microelectronics design, Analog, Digital and Mixed-Signal ASICs
- FPGA programming
- Electronics desing (Power electronics, front-end, read-out, DAQ, Control)
- Electronics production, test and verification
- Sub-systems assembly (mechanical design, cooling, integration)
- Commissioning and maintenance

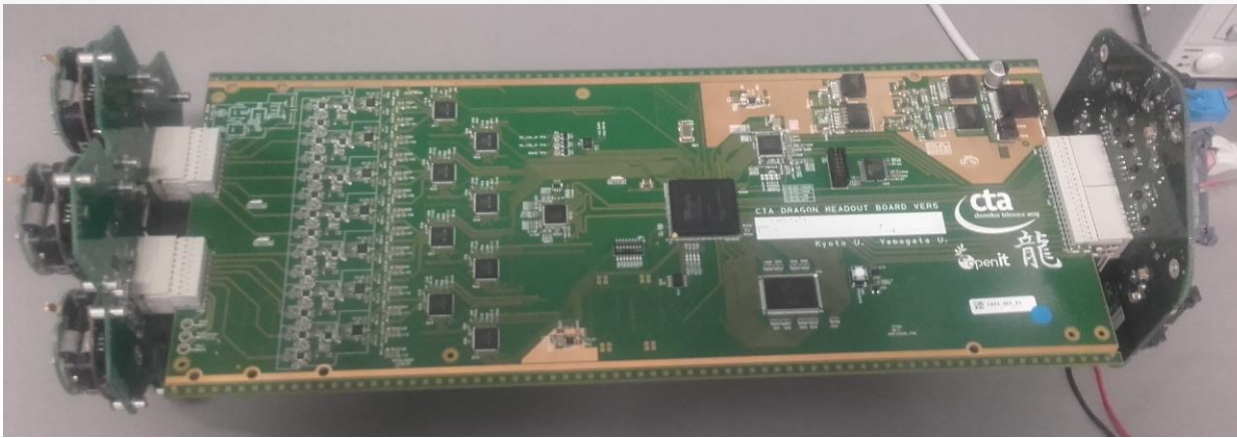


- 16 channels
- Selectable High Voltage from -20V to -40V (Very low ripple)
- 2 DRS4 sampling at 0.7 - 5 GSPS
- 2 ADC
- Altera Arria V FPGA for readout control, logic trigger, temperature control and on Board Digital Signal Processing
- Internal trigger with user-defined thresholds on any of the 16 channels
- Logic trigger section based on FPGA
- 16-bit DACs to generate all on-board control voltages
- USB interface for data readout and board control
- 25 GPIO for data readout and board control
- Internal timing calibration
- Internal voltage calibration
- 1Gb Flash Memory
- Peltier temperature controller

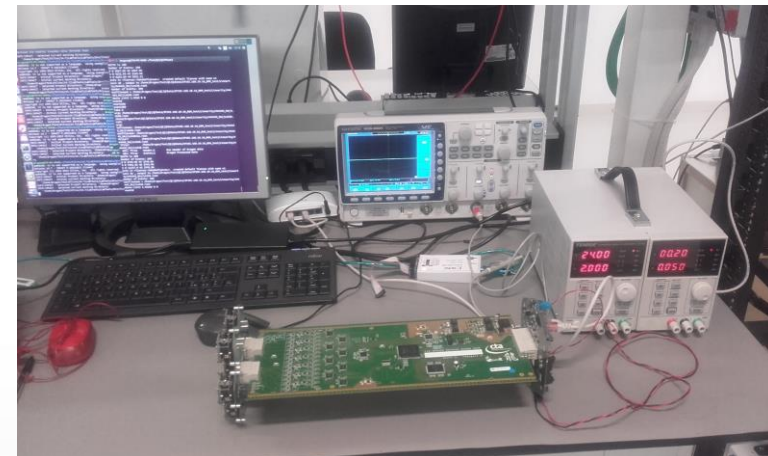








- Production and test of Dragon read-out board for the first LST prototype
- First pre-series just produced
- Test on-going
- 150 boards
- DRS-IV based





INDUSTRIAL
RAILWAYS

SITAEI
INDUSTRIAL

Nuovo progetto in sviluppo

- *Contatto diretto con ALTERA tramite Service Level Understanding*
- *Processamento segnali video*



Progetto:

- **diagnostica ferroviaria**

FPGA:

- **Altera ARRIA 10 10AX066K4F35I3**

Architettura/Funzionalità:

- **Controllo periferiche ed aggregazione dati:**
 - **Link PCIe – Gen 3.0**
 - **Memoria DDR3 256 MB@ 933MHz**
 - **NIOS II**
 - **Link 10GbE**
 - **Link CoaXPress @ 2.5Mbps**
- **Gestione periferiche:**
 - **Telecamere (2,5Mbps) in downlink e 20Mbps in uplink**
 - **Accelerometri**
 - **Giroscopi**
 - **Sensore di Temperatura**
 - **Interfacce RS485**

Nuovo progetto in sviluppo

- *Contatto diretto con ALTERA tramite Service Level Understanding*
- *Elaborazione dati da sensore CMOS*



Progetto:

- **Box Ottico**

FPGA:

- **Altera ARRIA 10 10AX066K4F35I3**

Architettura/Funzionalità:

- **Controllo sensore CMOS ed elaborazione dati**
 - **Memoria DDR3 256MB @ 933MHz**
- **Gestione periferiche:**
 - **Telecamere (2,5Mbps) in downlink e 20Mbps in uplink**
 - **Sensore immagini 4Mega-pixel @ 1000fps**
con interfaccia dati 80 link LVDS @532MHz in DDR
 - **Interfaccia GbE SGMII @ 1Gbps**



Progetti:

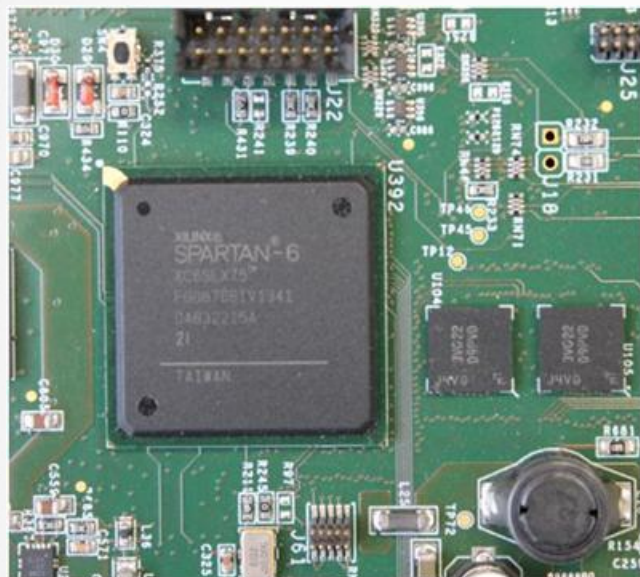
APPLICAZIONE Lidar

FPGA IN DIVERSITY:

- Sensore a Tempo di Volo (STV):
 - ALTERA Cyclone IV EP4CE10E22I7
- VB32
 - ALTERA Cyclone III EP3C55F484I7N;
 - LATTICE LFE2-50E LFE2-50E-7FN484C

Architettura/Funzionalità:

- STV: gestione impulso laser (4 ns) + misura tempo di volo
- VB32 - Architettura di south-bridge per il micro:
 - Interfacce di comunicazione verso sensore STV@20Mbps secondo protocollo RS485
 - Funzionalità di pre-processing sui dati ricevuti da STV (nuvola dei punti)
 - Funzionalità di debug verso interfaccia Wiznet @ 120Mbps
 - Interfaccia di acquisizione da encoders relativi e assoluti e aggragazione dati.



Progetti:

- HBD (Hot Box Detector)
- PMF (Portale MultiFunzione)

FPGA IN DIVERSITY:

- XILINX SPARTAN-6 XC6SLX75
- ALTERA Cyclone IV EP4CE75F2317N

Architettura/Funzionalità:

- Architettura di south-bridge per il micro:
 - Data Bus 32 bit, Addr Bus 23 bit
 - 4 link in Fibra Ottica (30 Mbps)
 - 2 porte Ethernet 10/100
 - 6 Interfacce RS485 (20 Mbps)
 - Memoria DDR2 512 Mb, 166 MHz
- Funzionalità HBD:
 - Acquisizione ed Elaborazione (Filtraggio FIR e sottocampionamento) segnale generato da 2 Sensori IR
 - Softprocessor: NIOS II e MicroBlaze
- Funzionalità PMF:
 - Generazione segnali vitali di sincronismo
 - Acquisizione 16 segnali di WS @ 250 KS/s
 - Elaborazione segnali per rilevazione asse (Filtri FIR) e calcolo velocità

**Progetto:**

- **BTM_DIAG_AV - BTM Diagnostico - Alta Velocità**

FPGA:

- **Altera Cyclone IV EP4CGX75CF23I7N**

Architettura/Funzionalità:

- **Architettura di south-bridge per il Modulo COMe:**
 - **Link PCIe – 250 MBps**
 - **5 link RS485 (10 Mbps)**
 - **Acquisizione segnali Odometrici**
 - **NIOS II**
- **Gestione dell'Antenna RSDD_AV**
- **Decodifica TLG Eurobalise**



Progetti:

- **SSB (SottoSistema di Bordo) SSC-SCMT BL3**
 - **BTM (Balise Transmission Module)**
 - **RSC_BACC (Blocco Automatico Correnti Codificate)**
 - **ODO (ODOmetria)**

FPGA:

- **Altera Cyclone II EP2C70**

Architettura/Funzionalità:

- **Architettura di co-processore per il micro**
- **Gestione delle periferiche dei vari sistemi**
- **Funzionalità BTM:**
 - **Modulatore e Demodulatore FSK**
 - **Decodifica Telegrammi Eurobalise**
 - **Memoria FIFO e Porta USB di debug**
- **Funzionalità RSC:**
 - **Acquisizione segnale RSC e rispettiva elaborazione**
 - **FFT 4096 punti**
 - **3 FIR: 200 taps, 50 MHz**
- **Funzionalità ODO:**
 - **Acquisizione segnali odometrici**

- Progettazione e produzione elettronica per
 - Astrofisica nello Spazio
 - Astrofisica a Terra
 - Altri progetti Spazio
 - Diagnostica e Segnalamento Ferroviario
- Progettazione con FPGA dai maggiori produttori
 - Altera
 - Xilinx
 - Microsemi
 - Lattice
- Circa 10 progettisti vhdl





Matteo M. Angarano
Sales and Marketing Manager
matteo.angarano@sitael.com

SITAEI S.p.A.
Via San Sabino, 21
70042 Mola di Bari (BA) – ITALY
Tel: +39 080 5321796
Fax: +39 080 5355048
www.sitael.com