OHB CGS

19/05/2016

Workshop su Applicazioni FPGA in ambito Astrofisico

SPACE SYSTEMS

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Use of Reprogrammable FPGA on EUCLID mission

EUCLID is a cosmology mission part of Cosmic Vision 2015-2025 whose prime objective is to study the geometry and the nature of the dark Universe (dark matter, dark energy).

The mission will investigate the distance-redshift relationship and the evolution of the cosmic structures by measuring shapes and redshifts of distant galaxies.

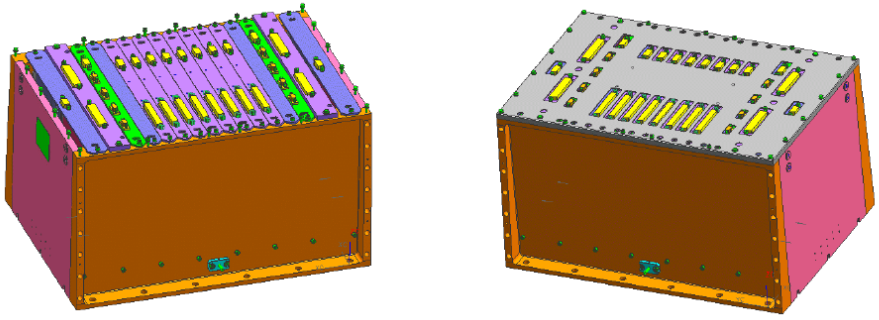
EUCLID space segment will be a spacecraft placed into an orbit around L2 with a coverage of 15,000 deg^2 in 6.25 years with step and stare observation strategy. Launch is planned for 2020.

EUCLID spacecraft will host 2 instruments:

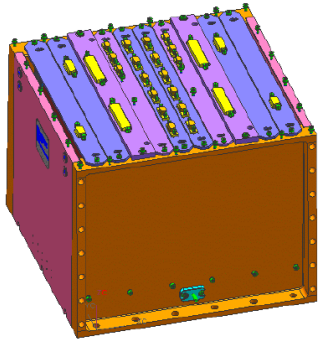
- NISP (Near Infrared Spectrometer Photometer)
- VIS (VISble imager)

CGS, in the frame of ASI contract, is in charge of the design of the Data Processing Units HW for both NISP and VIS as part of the Italian contribution to EUCLID mission in collaboration with the EUCLID Italian Science Team

- 1 CDPU unit for VIS
- 2 DPU/DCU units for NISP



NISP DPU/DCU units



VIS CDPU unit

Both units make large use of functions implemented in FPGA devices

Unit	FPGA devices	Types	Remark
CPDU	10	RTAX2000S	2x2 on SCS750F
DPU/DCU (single unit)	8	RTAX2000S	2x2 on SCS750F
DPU/DCU (single unit)	8	RT3PE3000L	

Microsemi RTAX-S FPGAs are based on anti-fuse technology, widely used in space application in both NASA and ESA mission because of the high level of immunity to radiation effects :

- SEL immune up to 117MeV/cm2/mg
- TID better than 200Krad
- F/F with TMR
- Logic SEU better than 1E-10 upset/bit/day on GEO

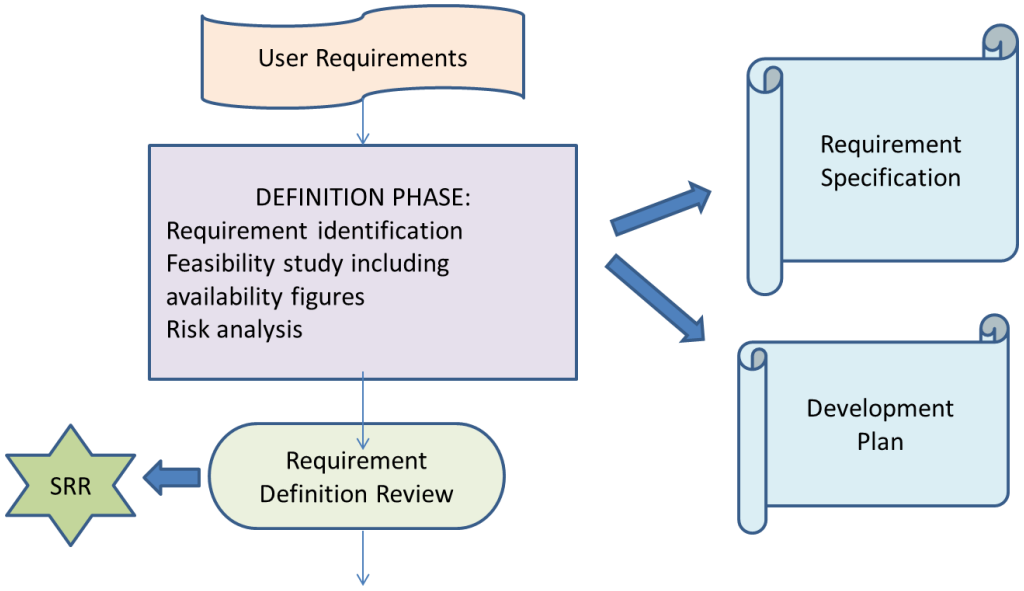
Microsemi RT3PE3000L FPGAs are based on commercial flash technology that exhibit lower level of radiation effects immunity but is reprogrammable :

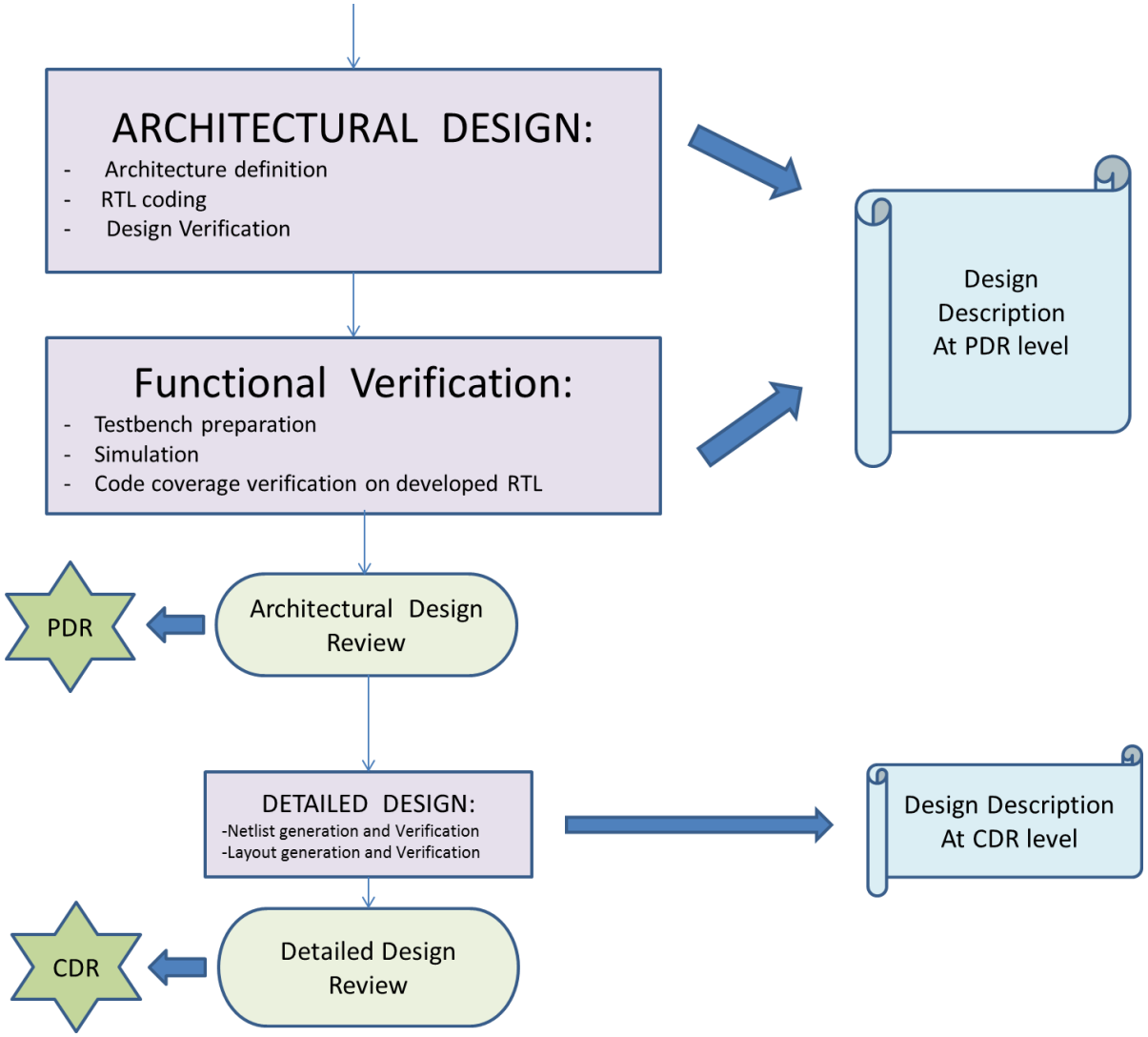
- SEL immune up to 68MeV/cm2/mg
- TID better than 30Krad (10% increase of propagation delay)
- No SEU effects on configuration cell
- D type F/Fs : Threshold 6 MeV-cm^2/mg, saturated x-section $2E^{-7}$ cm^2 per flip-flop

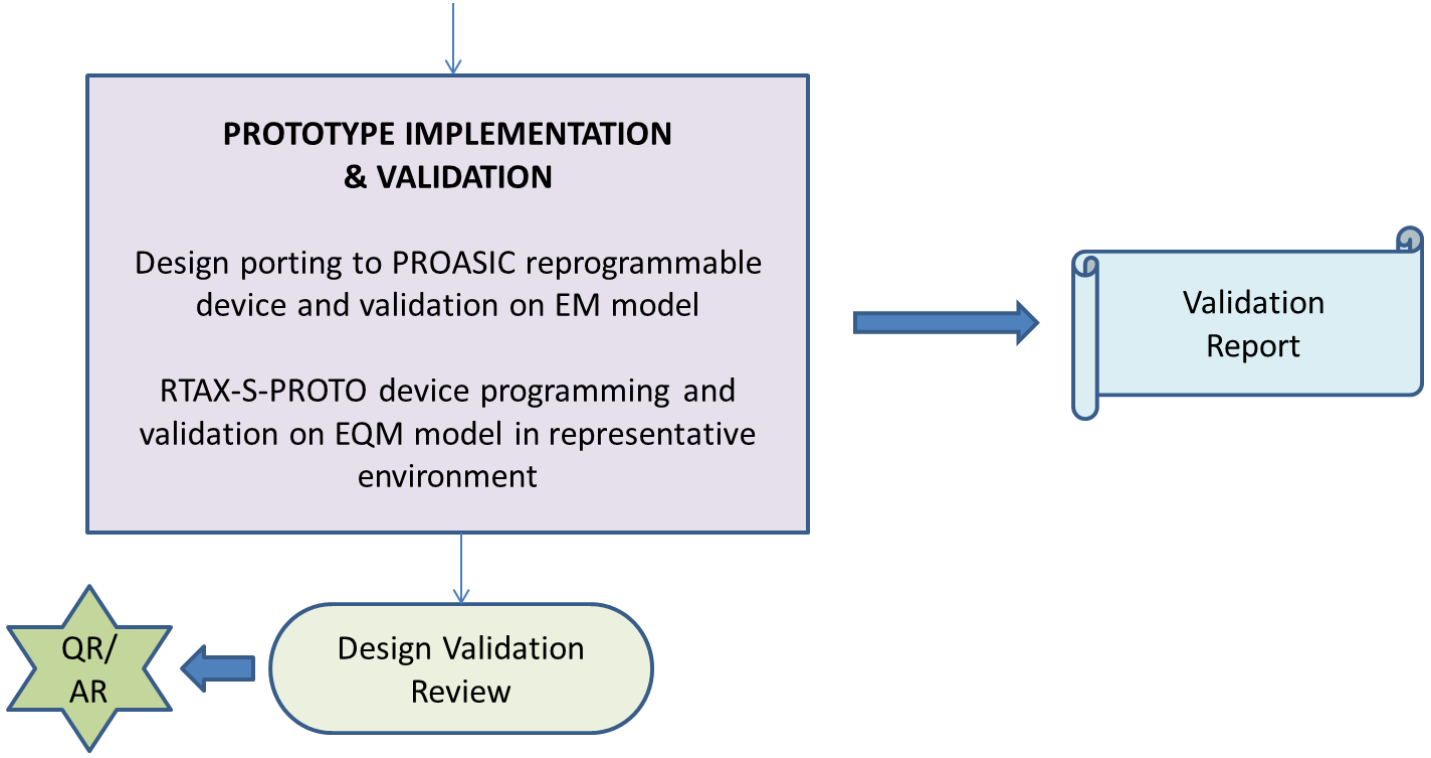
Radiation Hardening of FPGA design in RTAX-S for mission like EUCLID requires very limited effort

- EDAC on the internal SRAM in order to correct single errors
- Internal memory scrubbing for long term storage memory area
- Safe state machine

The design flow adopted in CGS is based on tailored ECSS-Q-ST-60-02C with the following steps

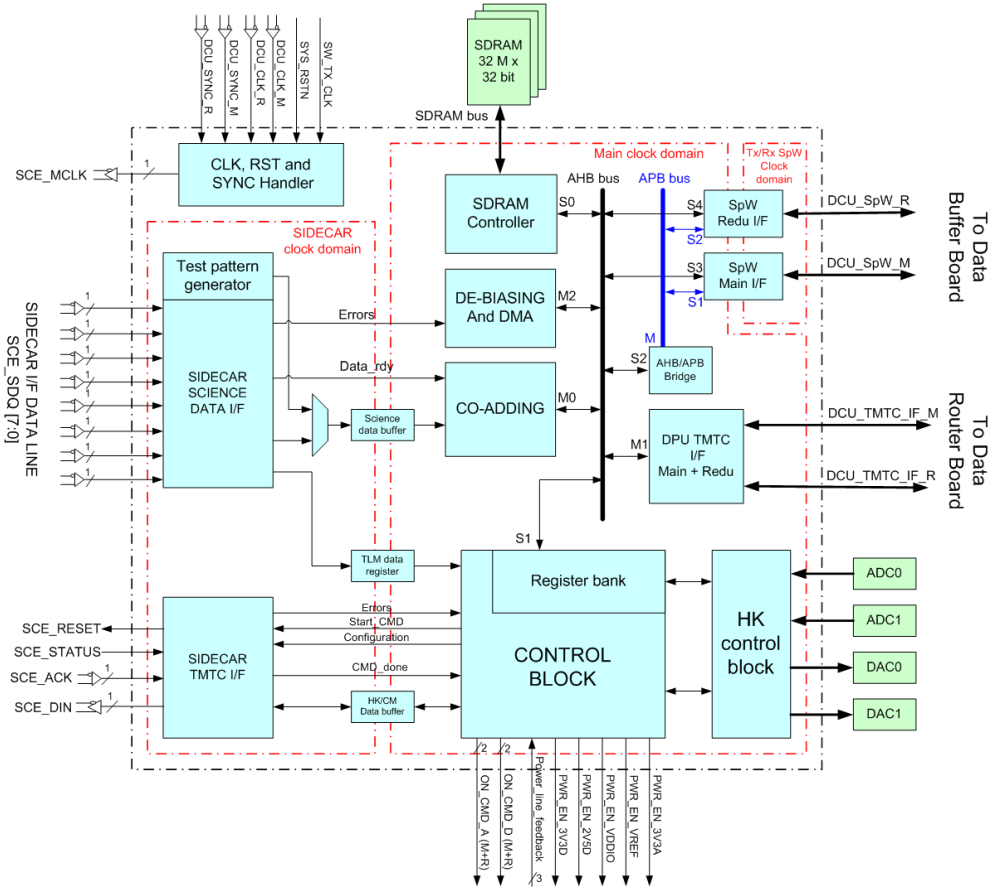



ARCHITECTURAL DESIGN:
- Architecture definition
- RTL coding
- Design Verification
Functional Verification:
- Testbench preparation
- Simulation
- Code coverage verification on developed RTL
Design Description At PDR level
PDR
Architectural Design Review
DETAILED DESIGN:
-Netlist generation and Verification
-Layout generation and Verification
Design Description At CDR level
CDR
Detailed Design Review


PROTOTYPE IMPLEMENTATION
& VALIDATION
Design porting to PROASIC reprogrammable device and validation on EM model
RTAX-S-PROTO device programming and validation on EQM model in representative environment
Validation Report
Design Validation Review
QR/ AR

Each DPU/DCU unit hosts 8 DCU boards, each board with 1 FPGA that implement

- Reception of data stream on 8x parallel lines and pixel de-serialization
- Buffering of the complete packet and CRC check
- Extraction of TLM from scientific data
- Coo-adding of pixels
- Averaging and formatting of the coo-added frames before transmission to the DBB



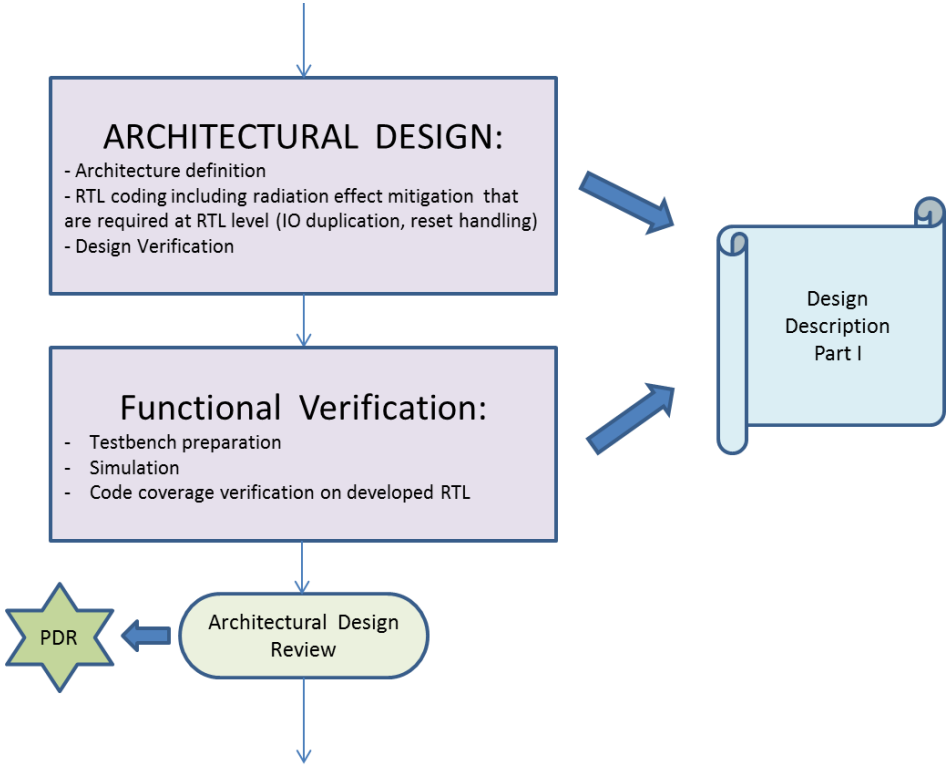
On EUCLID mission, for the FPGA implementing the interface with the detectors system, the use of a reprogrammable FPGA has been preferred for the following reasons:

- Request of *"maximum flexibility"* for the science team
- Lack of knowledge of the real behavior of the interface of the SIDECAR : unexpected behavior may require mitigation in the FPGA not known at the present time
- Risk of late modifications required on the FPGA design :
  - in case of use of RTAX FPGA, 16 identical FPGAs mounted on the 2 DPU/DCU could be impacted with high schedule/cost impact
  - RTPROASIC will allow the modification of the design via JTAG without opening the DPU/DCU unit and changing the device

Radiation Hardening of FPGA design in RT PROASIC requires not negligible effort

- EDAC on the internal SRAM in order to correct single errors
- Internal memory scrubbing for long term storage memory area
- Safe state machine
- Radiation Hardening at RTL level
- Radiation Hardening of the I/Os
- SET effect evaluation
- TMR of F/Fs implemented in the netlist
- Radiation aware placement
- Gard Gates introduction where necessary

The standard FPGA design flow is modified with the introduction of Radiation Mitigation activities



At RTL level

- Implementation of local reset for the different functional blocks that can be reset before use by the SW or by the internal FPGA logic avoiding error accumulation
- Implementation of independent controls for critical I/Os
- Duplication of critical I/Os

Radiation Hardening of the I/Os

- Identification of the criticality of the I/Os of the FPGA and need for mitigation
- Estimation of the probability of error due to radiation effects on the I/Os in EUCLID environment
- Mitigation definition : duplication or triplication of the I/O in different banks, external filtering, …
- Compatibility with Signal integrity on the board
- Compatibility with the available free pins on the FPGA

FPGA NAME	Description	Effect in case of SET	Criticality 1 = maximum, 5 = minimum	Mitigation proposed on the I/O	required # PIN
science_data0	Science I/F data bit0	Input data error, detected by CRC and not used in the computation of the coadding.	5	None	1
SCE_RESET_CMD_N	Reset command for the SIDECAR, active low. Both reset commands shall be low in order to reset the SIDECAR.	SIDECAR reset, loss of ASIC internal biasing	1	I/O duplication on 2 different banks. Single error will not cause the SIDECAR reset	2
SCE_STATUS_N	When high signals that an internal error has been detected by the SIDECAR	False internal error indication in the science data packet. This signal is sampled once every group, so probability of error is very low	4	None	1
UART_RX_MAIN	RS485 MAIN UART input	Possible communication error with the DRB. Message will be discarded by parity check or higher level protocol check (CRC)	5	None. Sampling time of the IF is 800KHz, I/F is rarely used, probability to cacth the pulse is very low	1
ON_VREF	Turn on the DC/DC converter of the vref isolated section. Both command shall be low to turn off the DC/DC	SIDECAR power-off, loss of ASIC internal biasing	1	I/O duplication on 2 different banks	2
ON_VDDA	Turn on the DC/DC converter of the VDDA isolated section. Both command shall be low to turn off the DC/DC	SIDECAR power-off, loss of ASIC internal biasing	1	I/O duplication on 2 different banks	2
SDRAM_DATA0	SDRAM data line	Transient anomaly on the SDRAM I/F can cause data loss.	3	None. To be evaluated the error rate induced by SET on this functional block	1

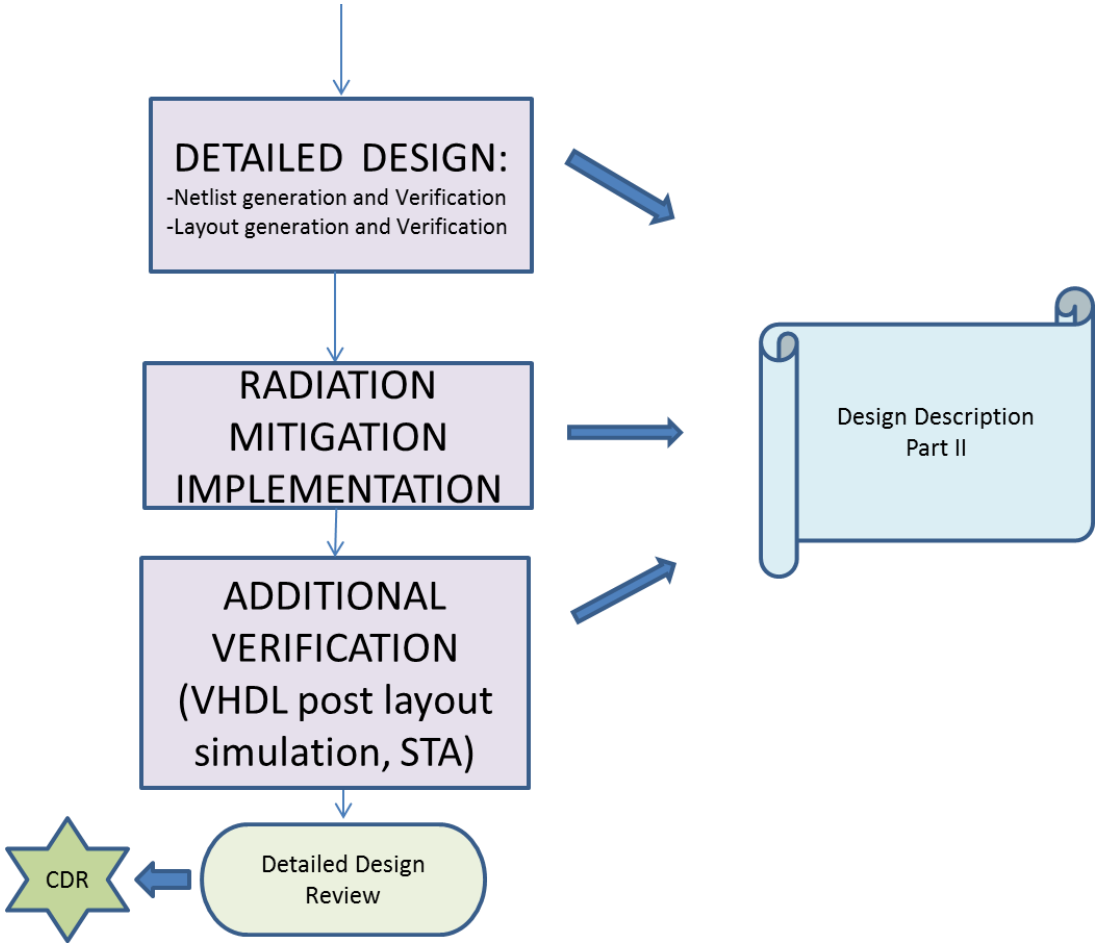
The analysis has been performed with CREME using the cross sections derived from “New methodologies for SET characterization and mitigation of Flash based FPGAs”, TNS-00477-2007.R2.

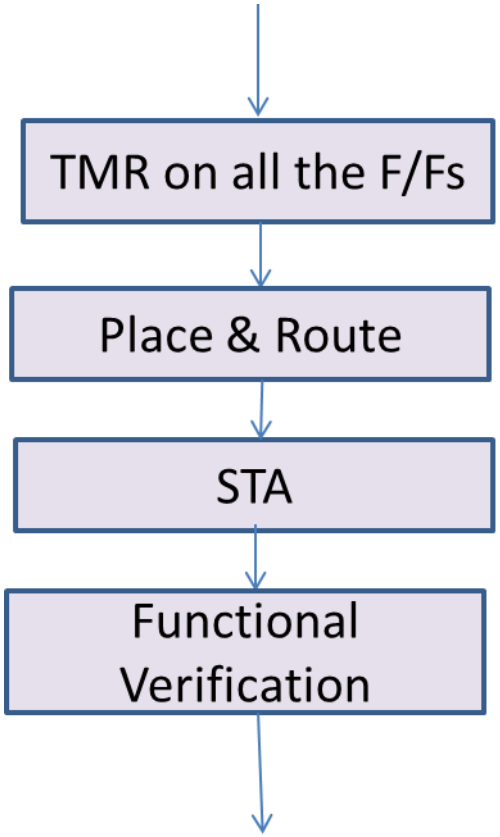
Type of error	Error signature	Remarks
Type 1 : SET on the IO channel	Transient on the output or input	SET generated internally that is able to propagate up to the FPGA output. Will be analyzed by POLITO with SETA on the actual FPGA netlist
Type 2 : SET observed for short time involving an entire (and only one) IO bank	IO bank disabled for few ns	The IO bank has a global enable signal that is driven by combinatorial logic + latch. If the SET involves the combinatorial logic, the bank is disabled for few ns
Type 3 : SET observed for long time involving an entire (and only one) IO bank	IO bank disabled for about 250 ns	The SET involves the latch. The circuit that disables the I/Os during power-on in order to avoid high inrush current is triggered and the entire bank stay disabled for about 250 ns, depending on the frequency.

Predicted error rate due to the I/Os on EUCLID mission considering 16 FPGAs and implementation of the mitigation is

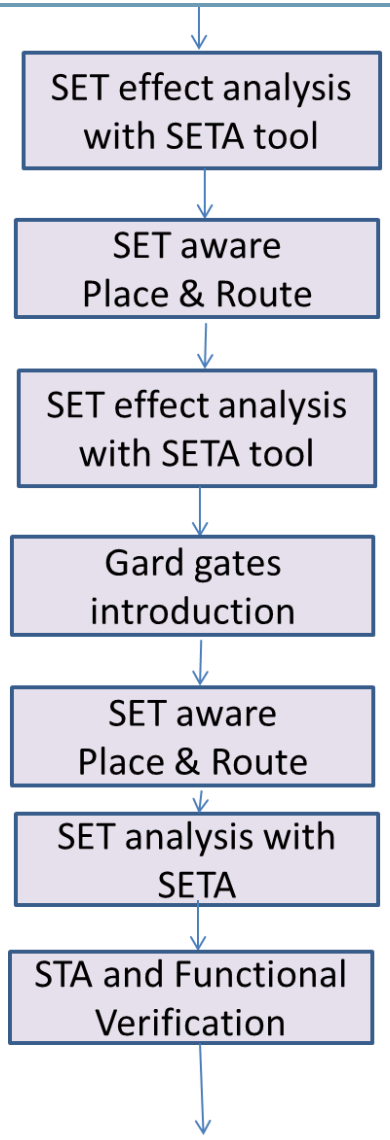
Event	NISP data processing Event rate [#/year]	Mean Time between events [years]
SIDECAR Reset or Power off	9,44E-03	105,91
Data loss	1,92E-02	52,18

Before CDR Radiation Hardening on netlist is implemented





- TMR on all the F/Fs is implemented starting from the VHDL with synthesis tool Synplify as baseline
- Place & Route of the FPGA is performed with Microsemi Designer
- Static Timing Analysis
- Functional verification with testbench on the post-layout netlist



- Definition of SET to injected in the simulation
- Simulation with SETA tool developed by POLITO to identify the F/Fs and the I/O that are sensitive to the SET
- Perform SET aware place & route to minimize the effect of SET without logic resources use
- Identify the nodes that are critical and perform gard gates insertion in the netlist
- Perform SET aware place & route
- Verify the design with SETA tool for effectiveness of SET filtering
- Perform final FPGA verification checking the timings with STA and performing functional verification with VHDL simulation

Validation of the FPGA design with RT PROASIC – proto device on the EM at ambient temperature and EQM model in representative temperature range